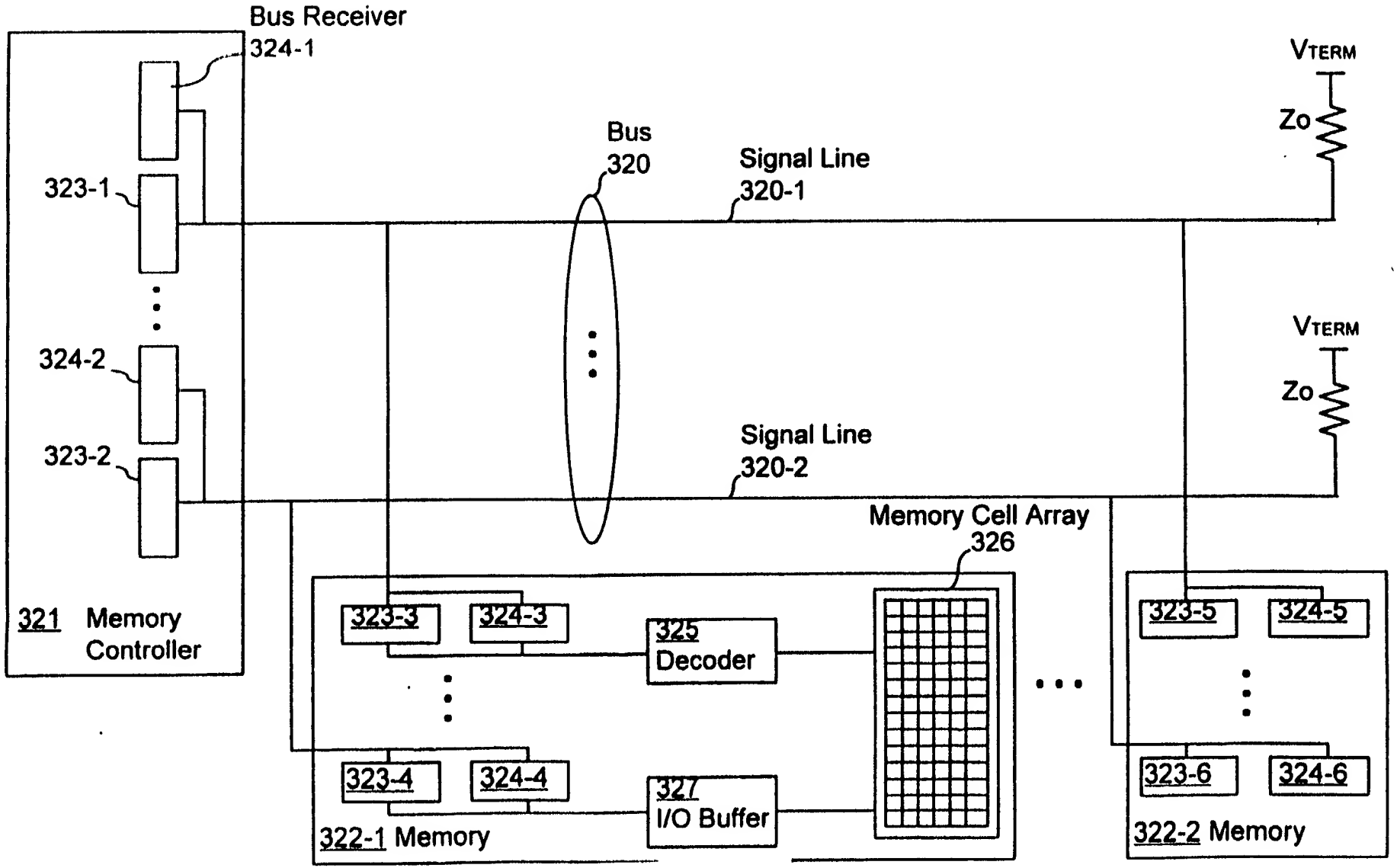


FIG. 1

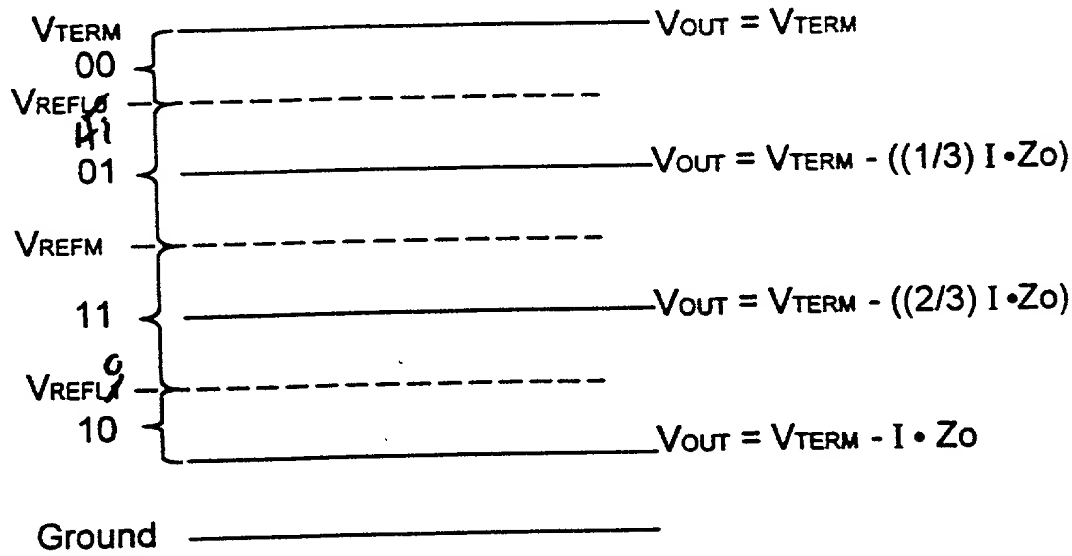

VTERM
00
VREFLO
01
VREFM
11
VREFL
10
Ground
VOUT = VTERM
VOUT = VTERM - ((1/3) I •Zo)
VOUT = VTERM - ((2/3) I •Zo)
VOUT = VTERM - I • Zo

FIG. 2

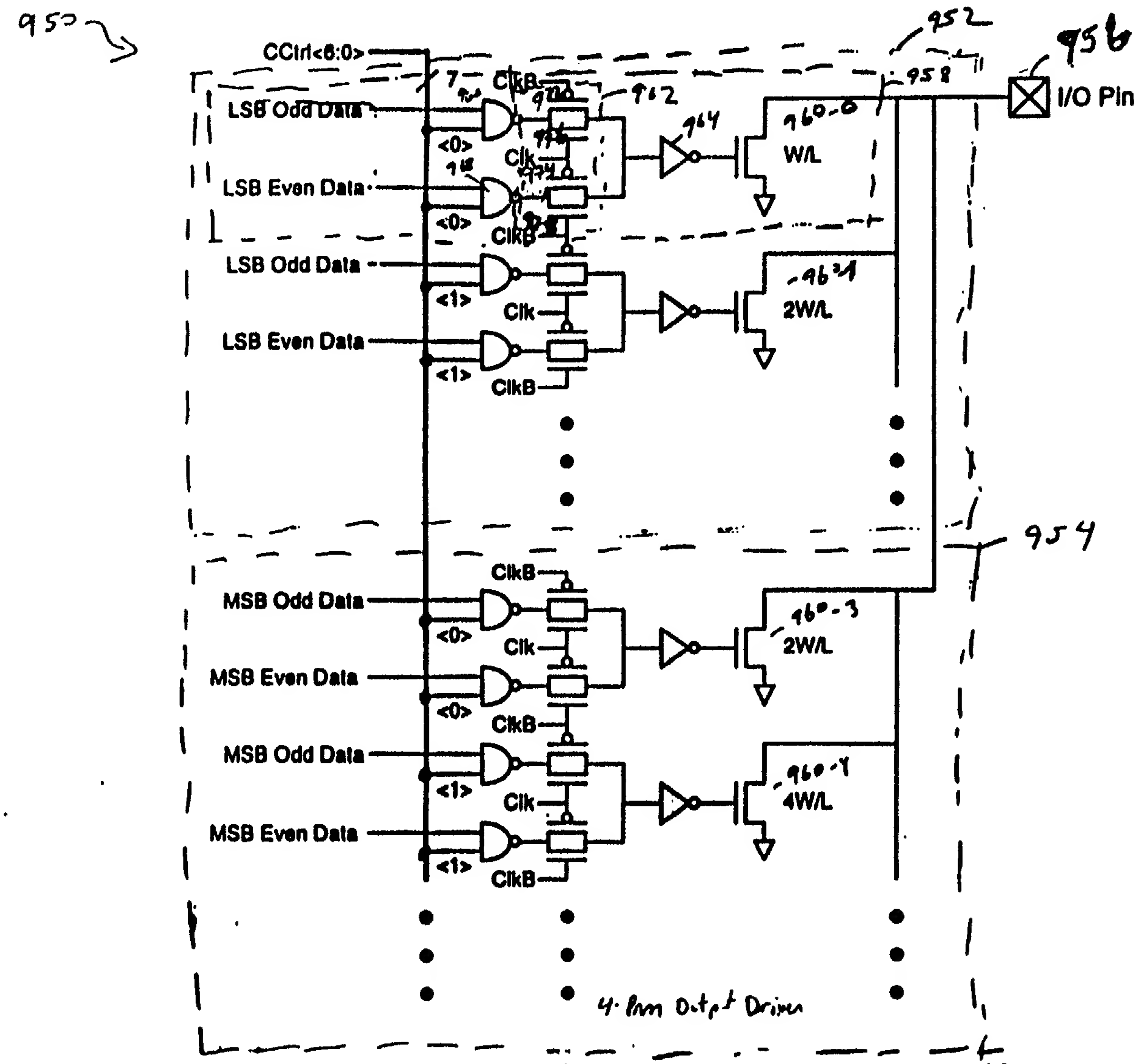

950
CCtrl<6:0>
LSB Odd Data
LSB Even Data
LSB Odd Data
LSB Even Data
MSB Odd Data
MSB Even Data
MSB Odd Data
MSB Even Data
<0>
<1>
Clk
ClkB
W/L
2W/L
4W/L
I/O Pin
952
954
956
958
962
964
4-Pam Output Driver

FIG. 3A

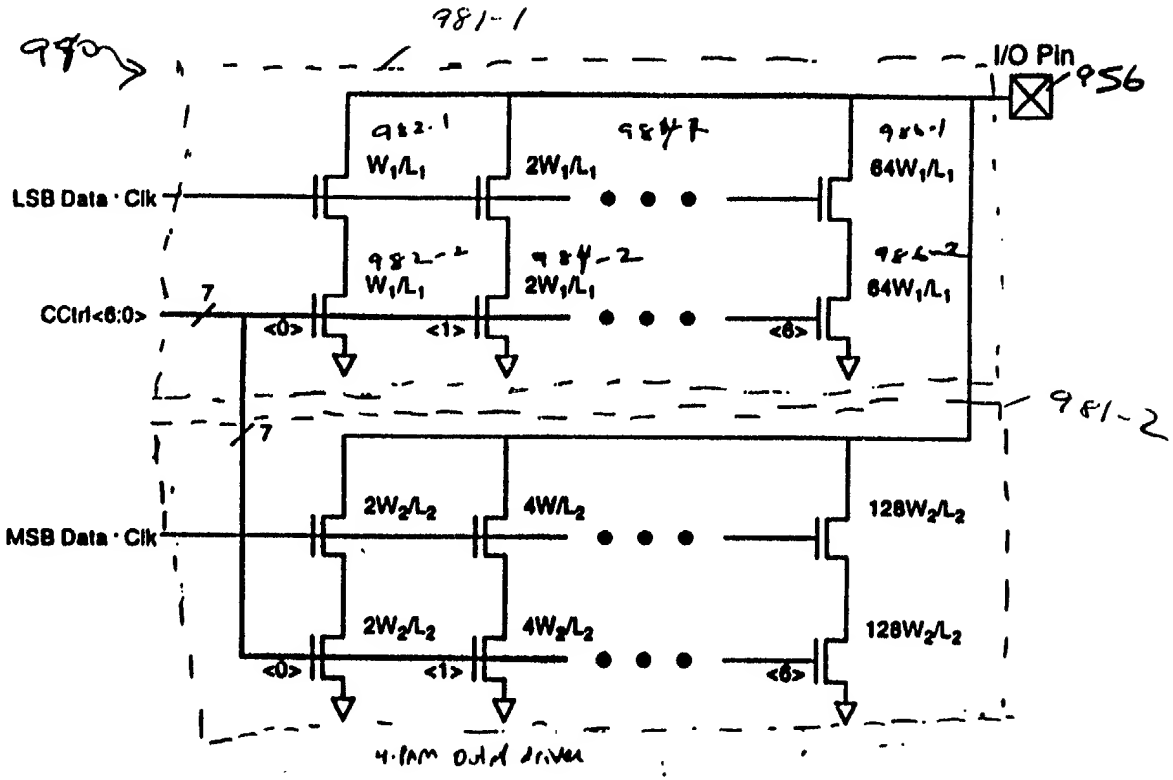

981-1
990
I/O Pin
956
LSB Data · Clk
CCtrl<6:0>
7
<0>
<1>
<6>
W1/L1
2W1/L1
64W1/L1
981-2
MSB Data · Clk
2W2/L2
4W/L2
128W2/L2
4W2/L2
4-bit odd driver

FIG 3B

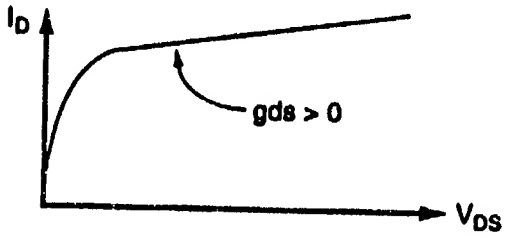


FIG 4A

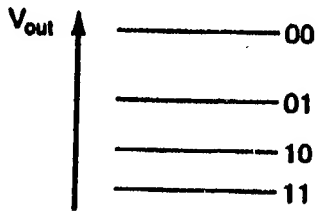


FIG. 4B

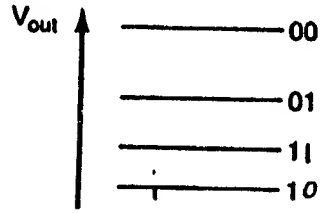
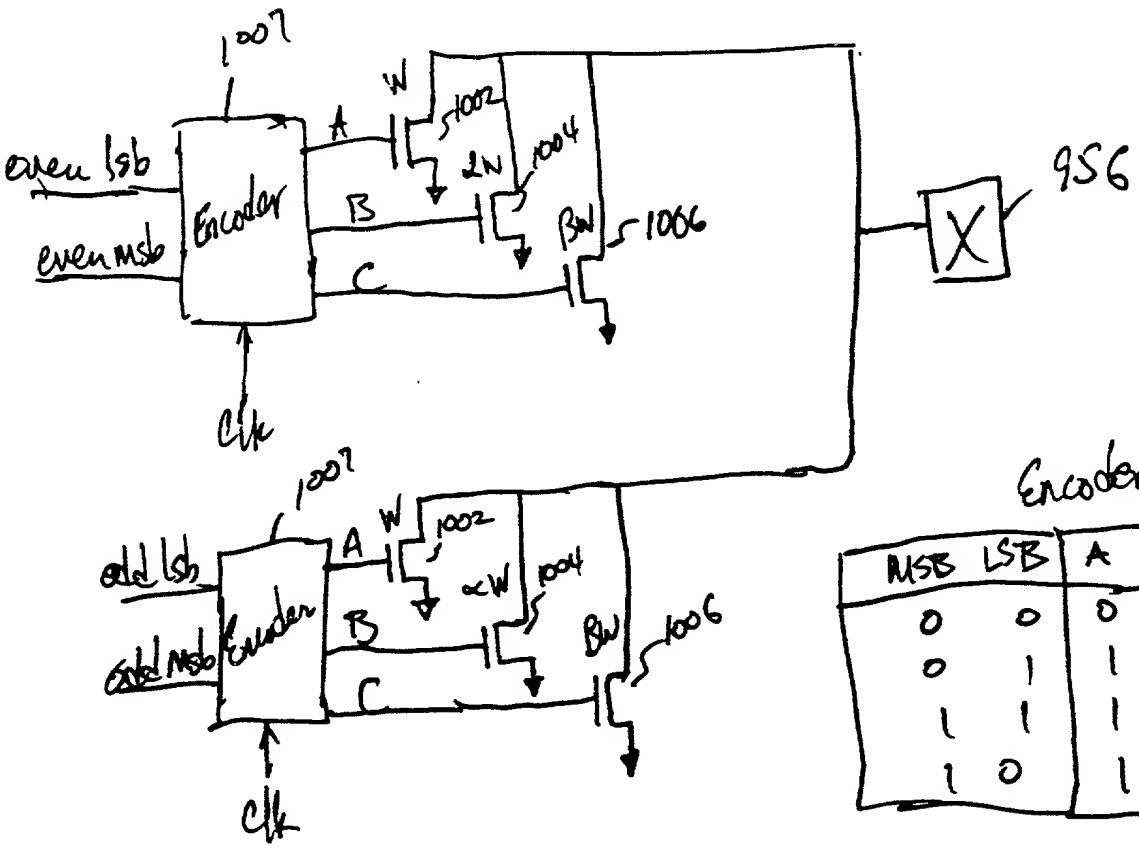


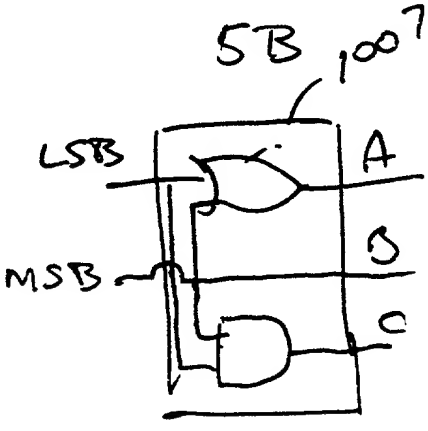
FIG. 4C

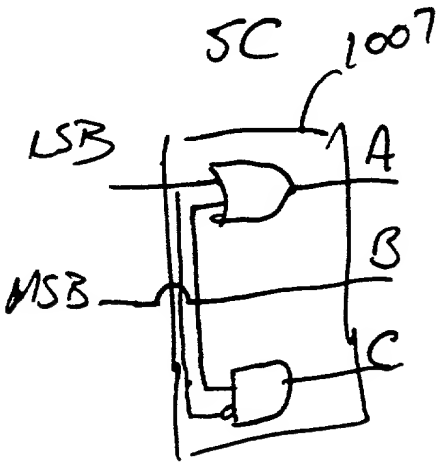
FIG. 5A

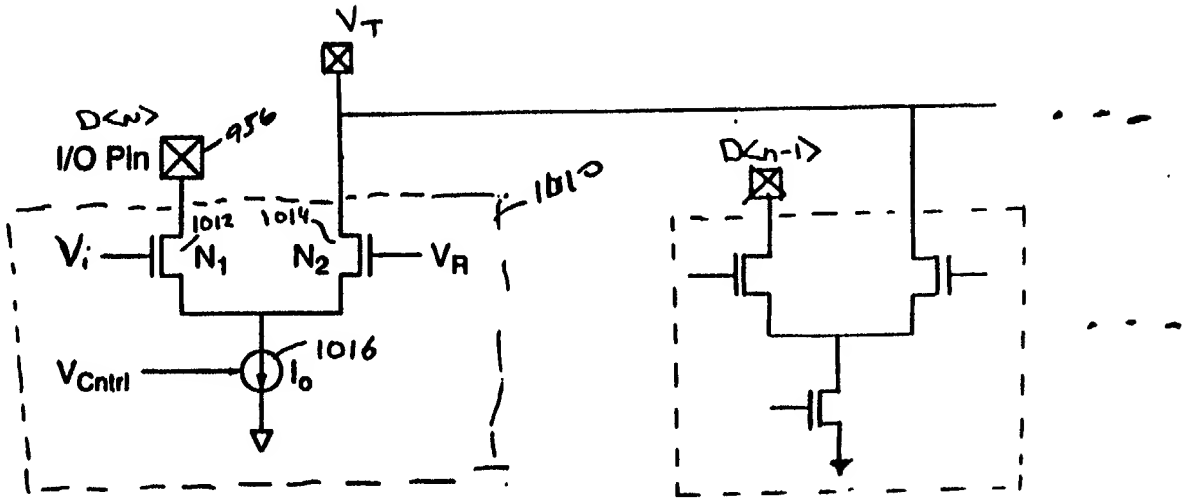


Encoder logic

MSB	LSB	A	B	C
0	0	0	0	0
0	1	1	0	0
1	1	1	1	0
1	0	1	1	1







circuit to Reduce Switching Noise

FIG 6

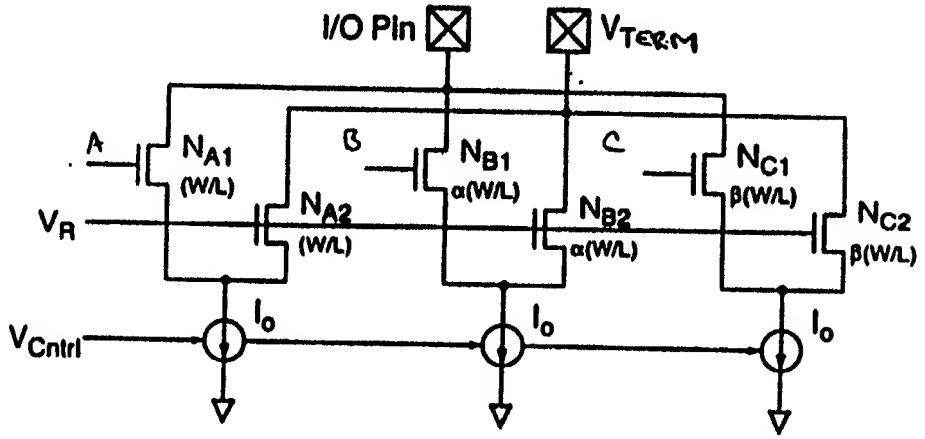
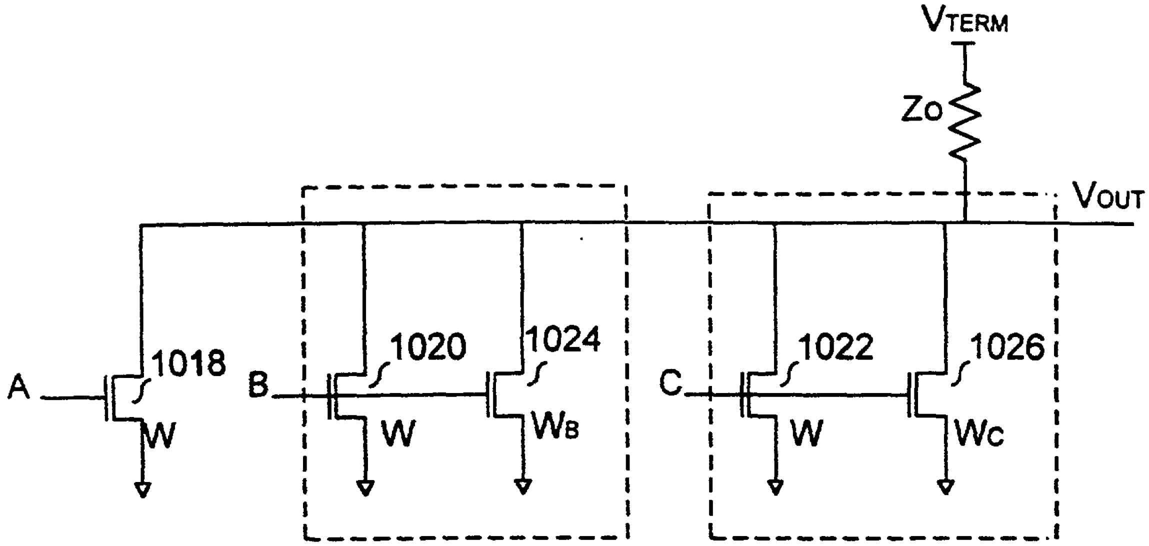
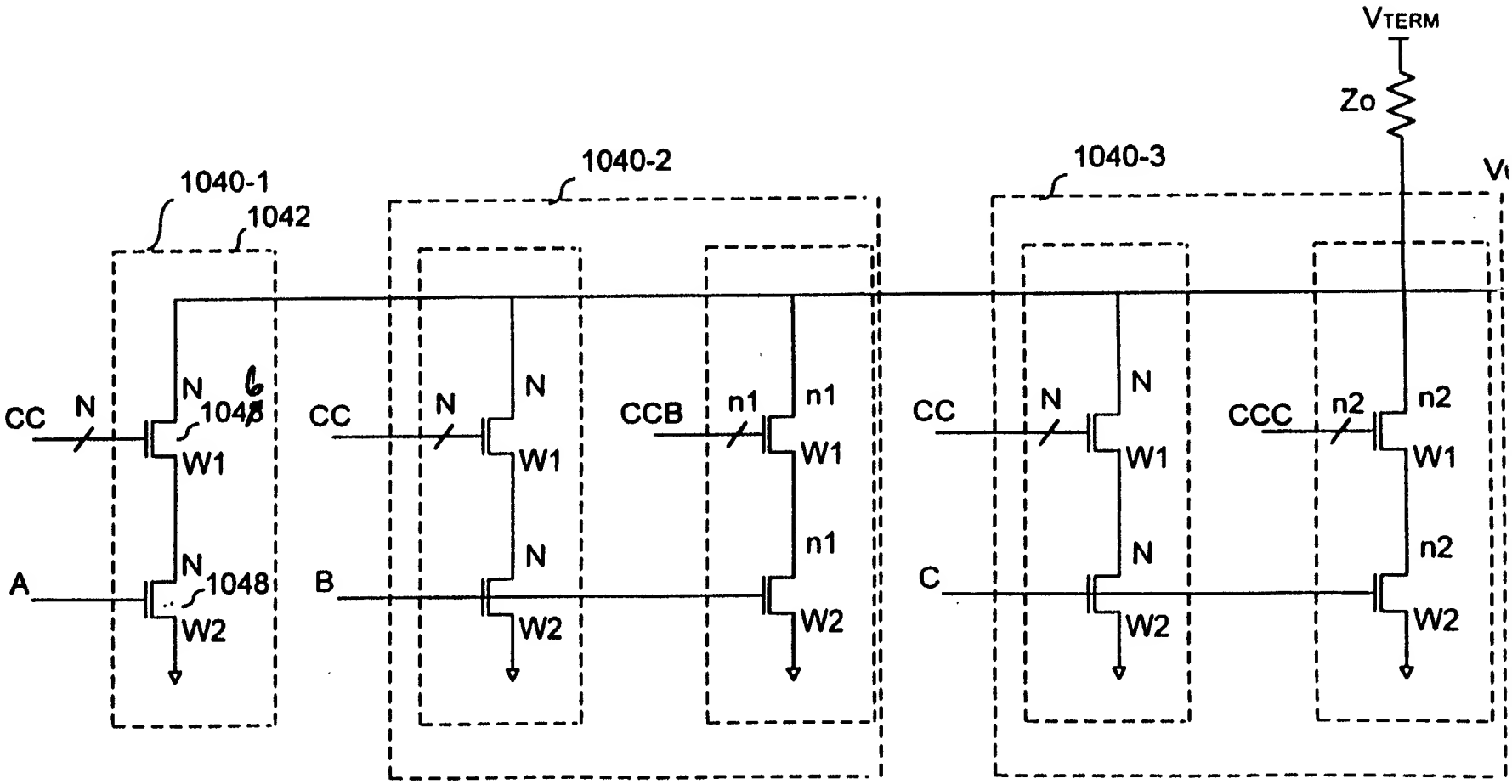


FIG. 7



GDS Compensated Multi-PAM Output Driver

FIG. 8



GDS Compensated Multi-PAM Output Driver with Current Control

FIG. 9A

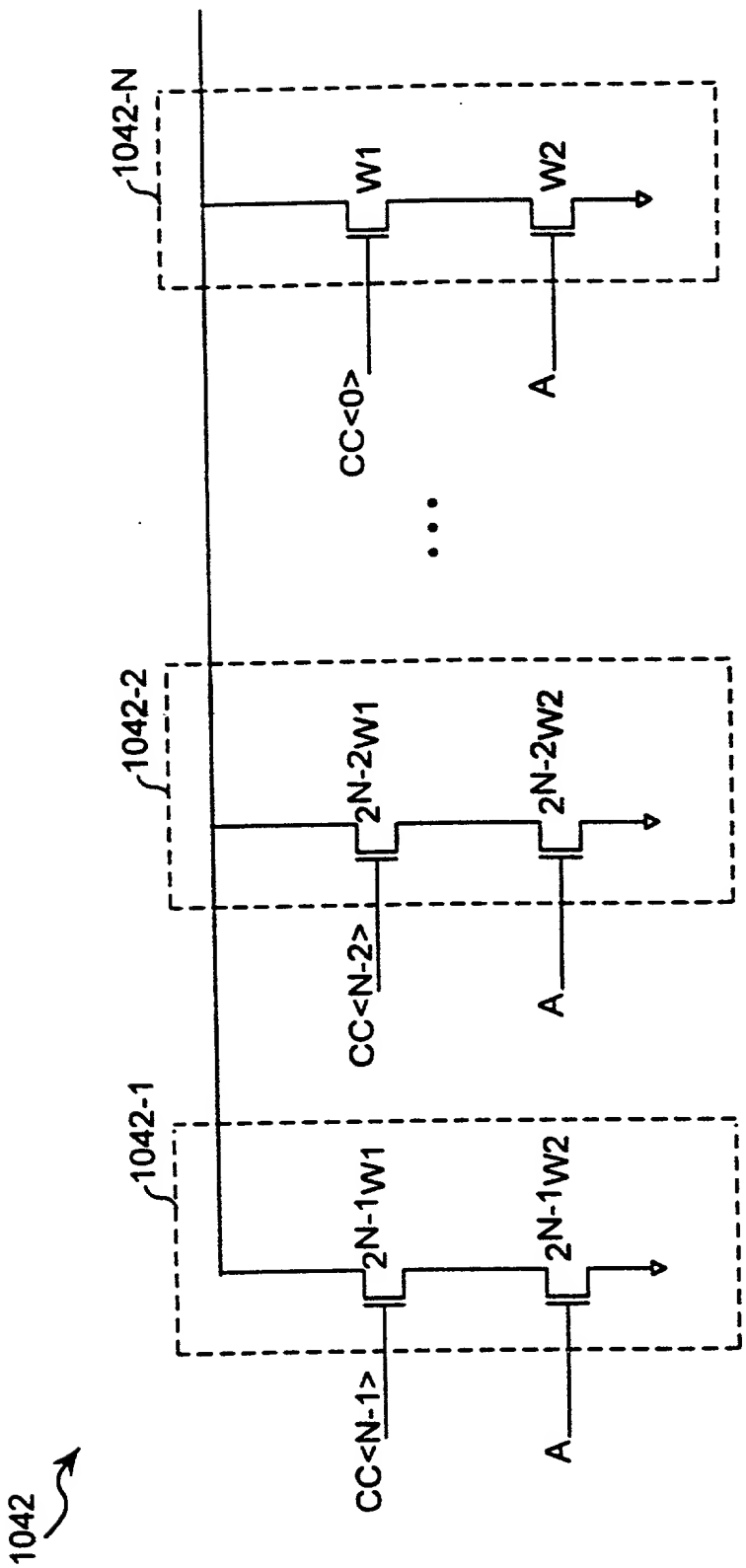

1042
1042-1
1042-2
1042-N
2N-1W1
2N-1W2
2N-2W1
2N-2W2
W1
W2
CC<N-1>
CC<N-2>
CC<0>
A
A
A

FIG. 9B

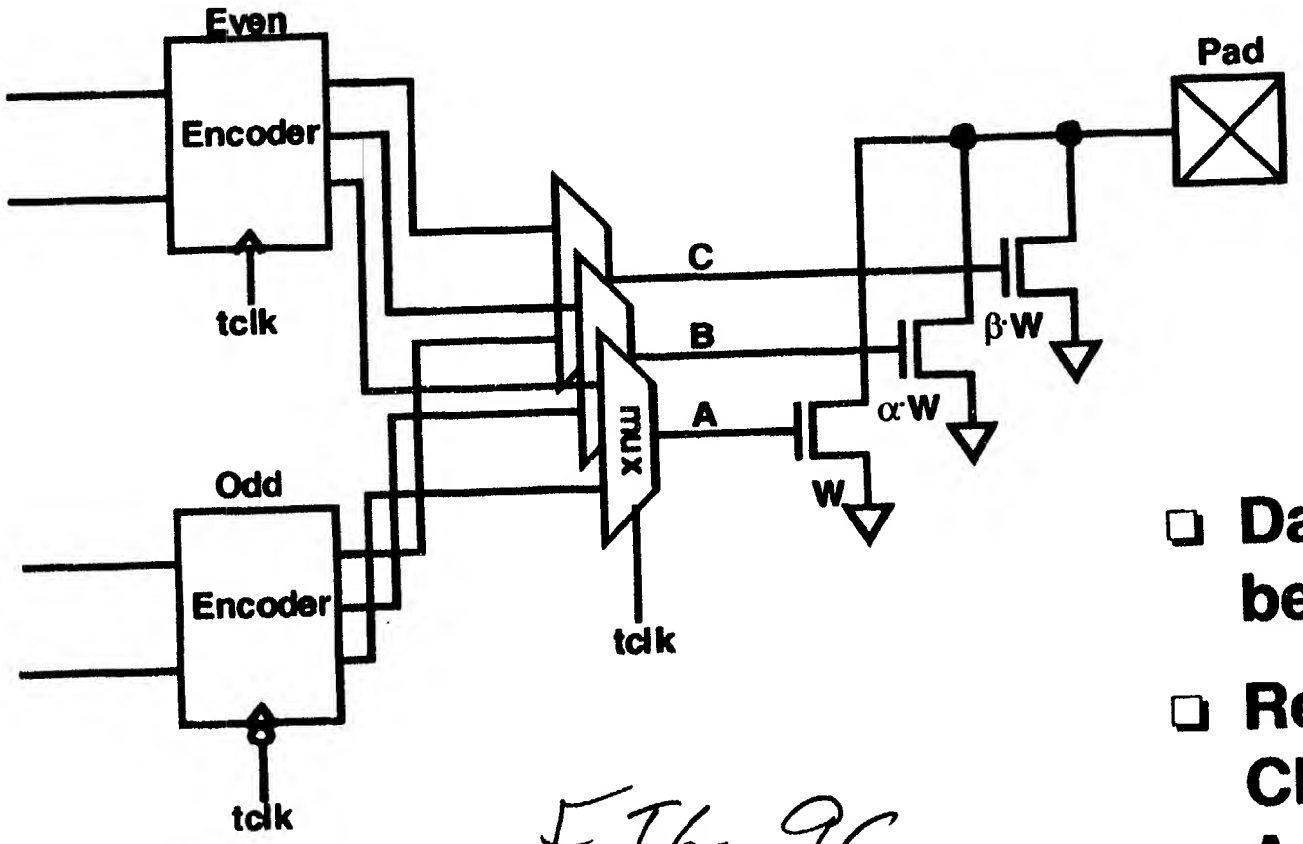
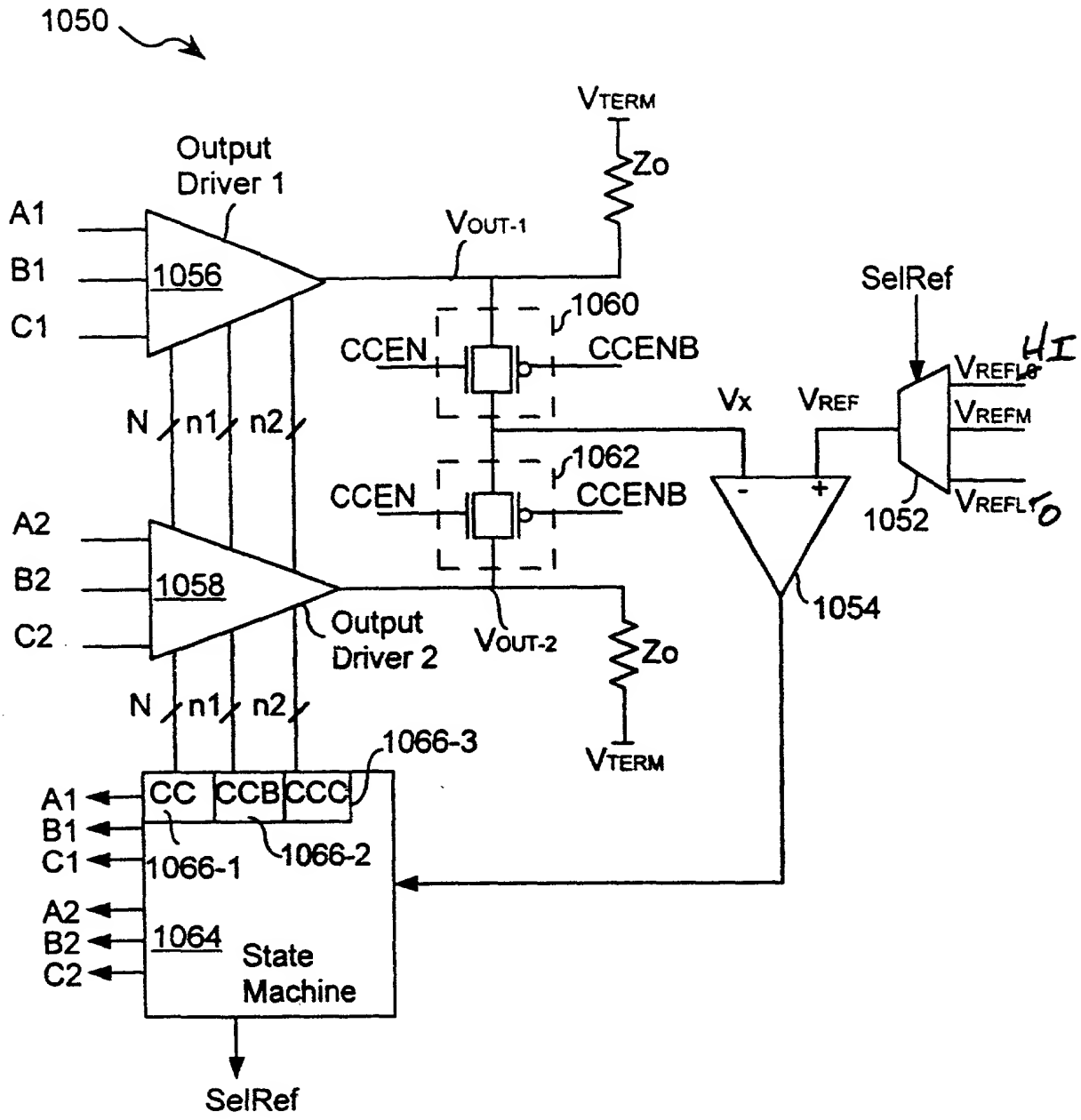


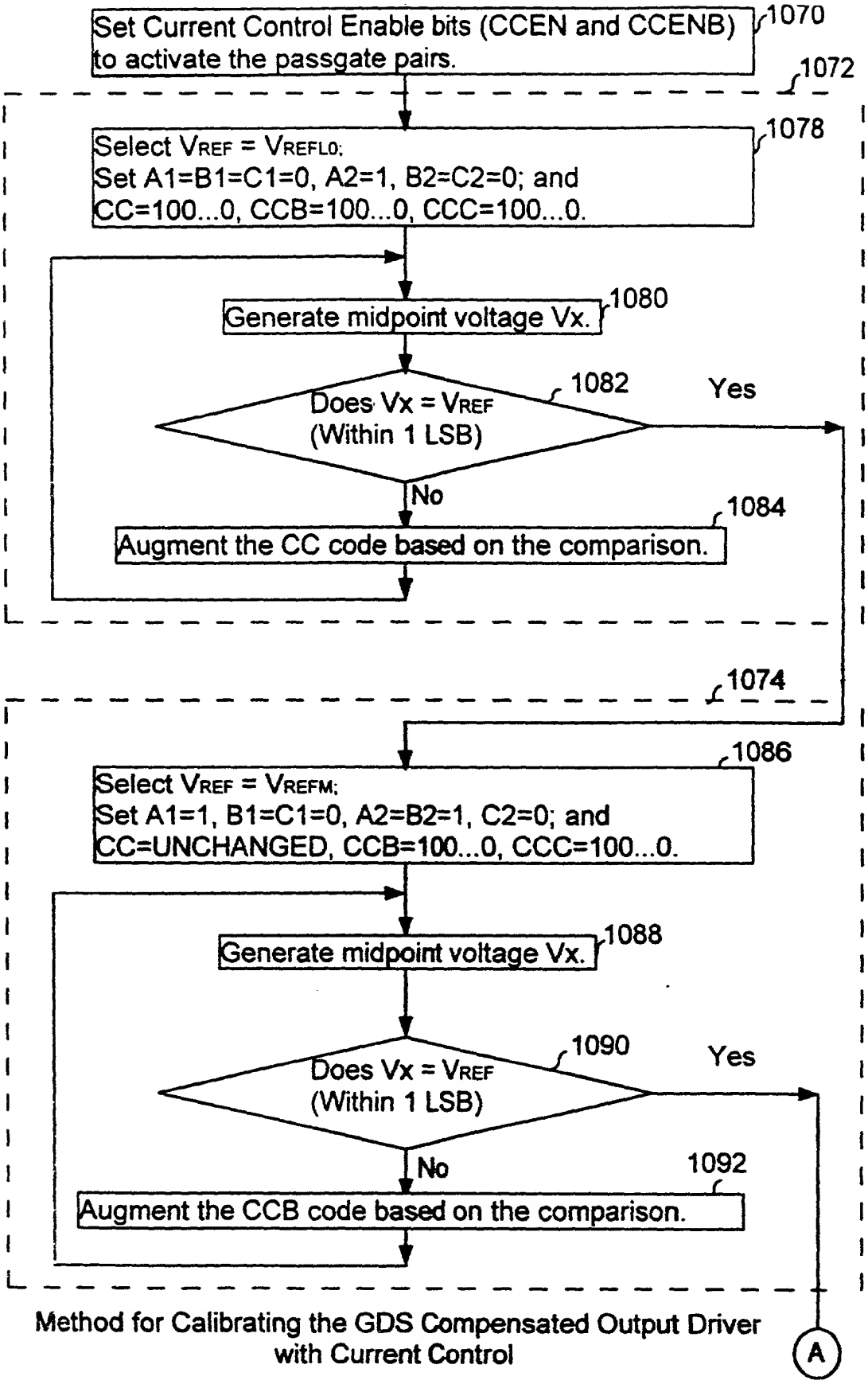
FIG. 9C

- Data muxed before pad
- Requires running CMOS signals A,B,C @ full frequency



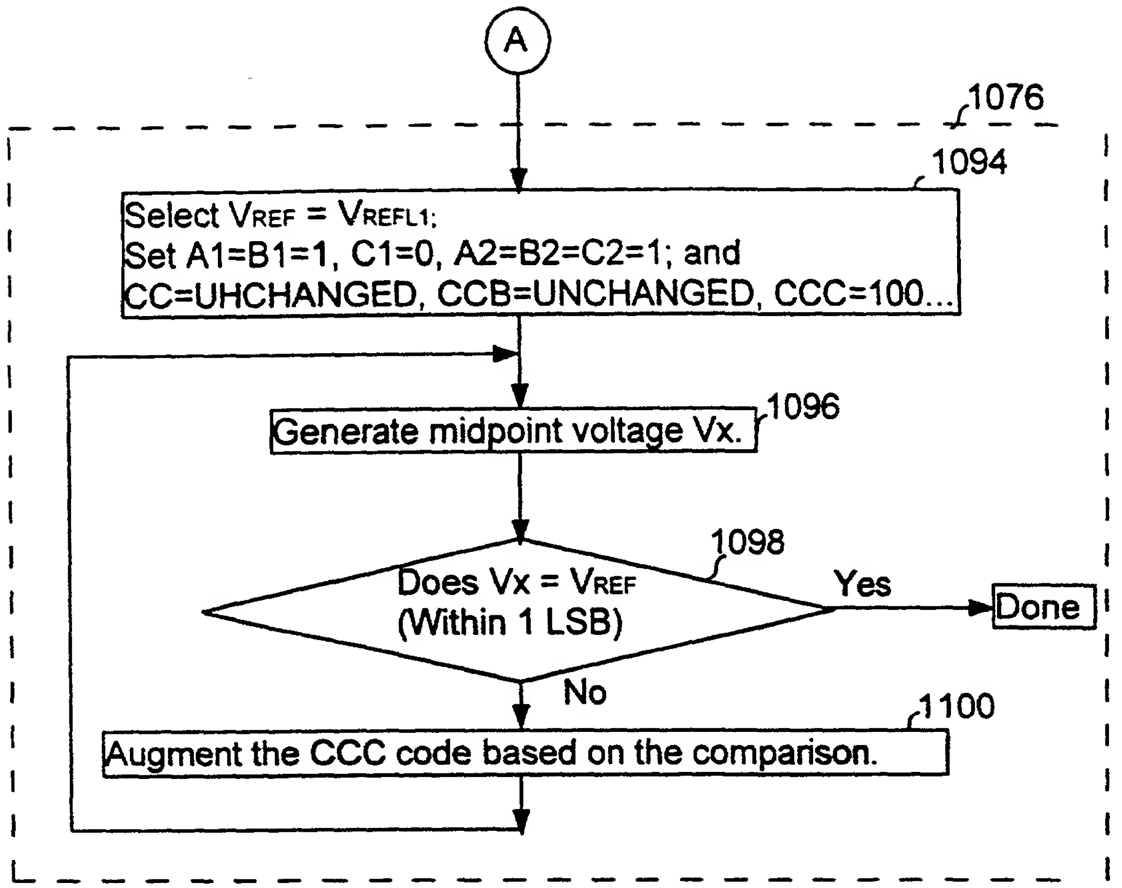
Circuit for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 10



Method for Calibrating the GDS Compensated Output Driver with Current Control

FIG. 11A



Method for Calibrating the GDS Compensated Output Driver
with Current Control

FIG. 11B

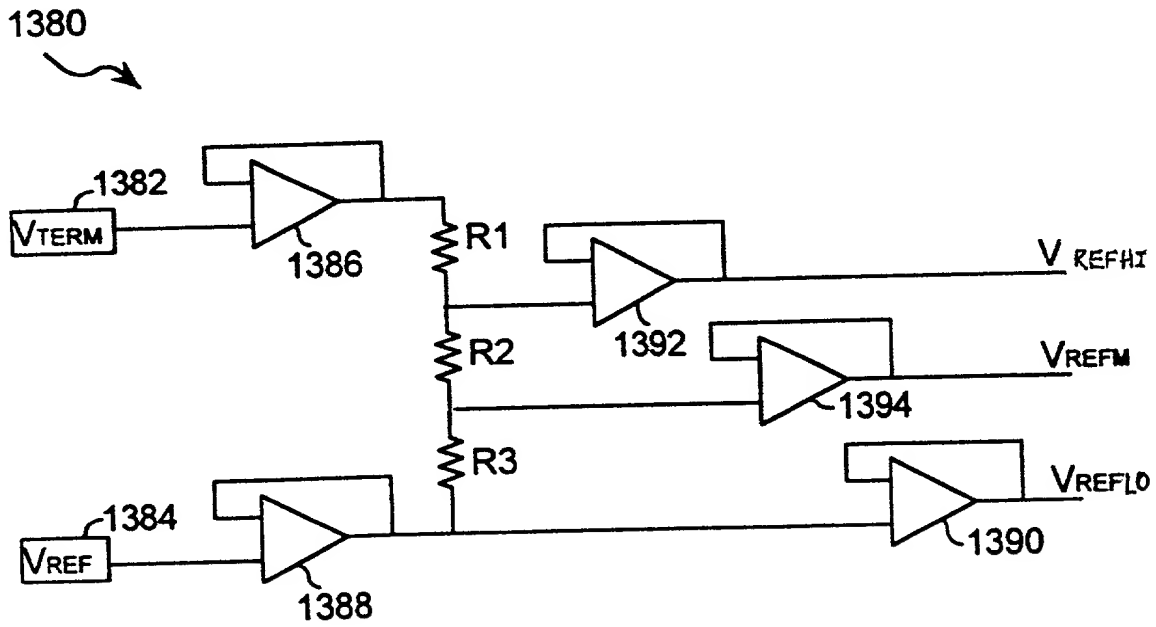

1380
1382
VTERM
1386
R1
V REFHI
1392
R2
VREFM
1394
R3
VREFLO
1390
1384
VREF
1388

FIG. 12

FIG 13A

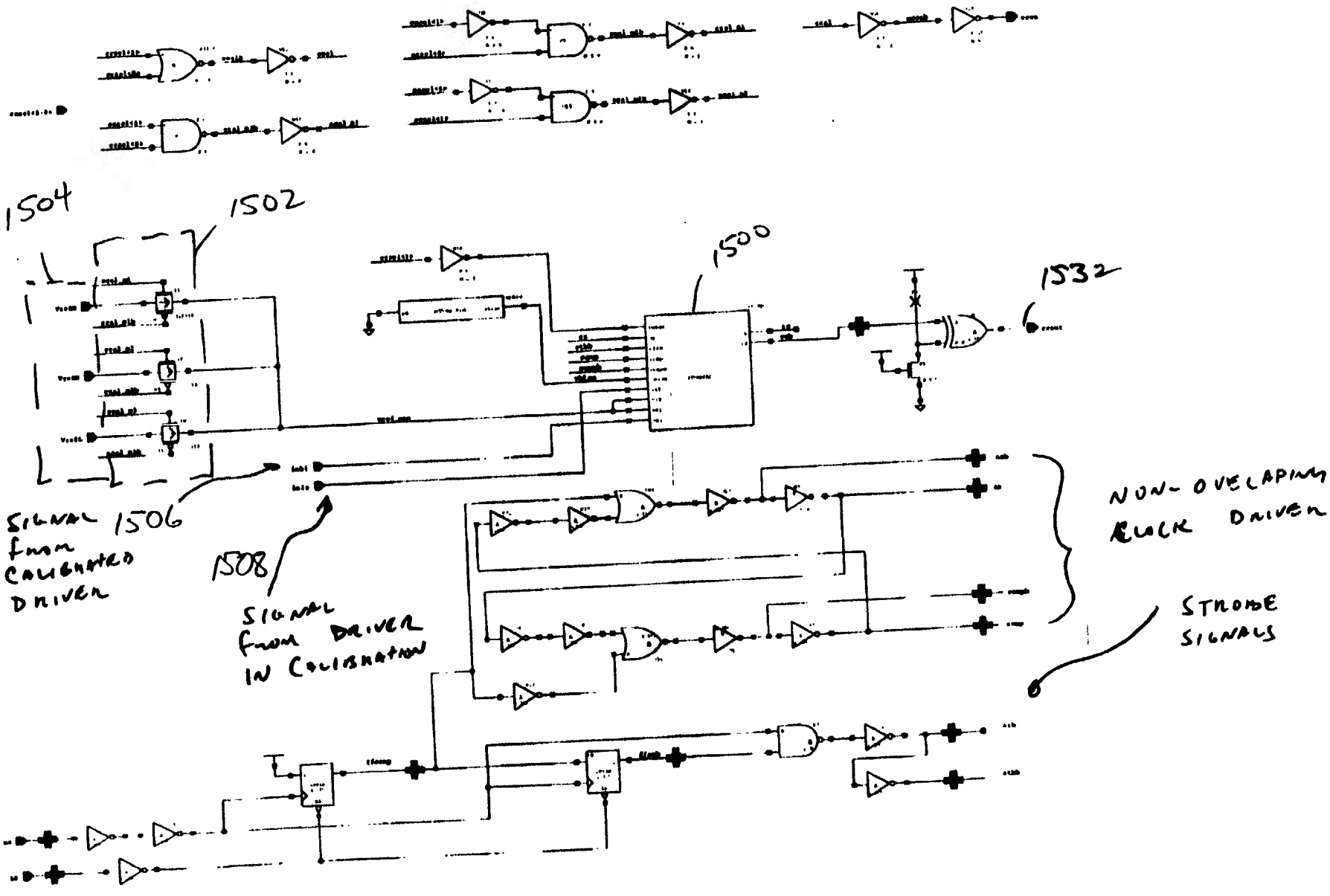
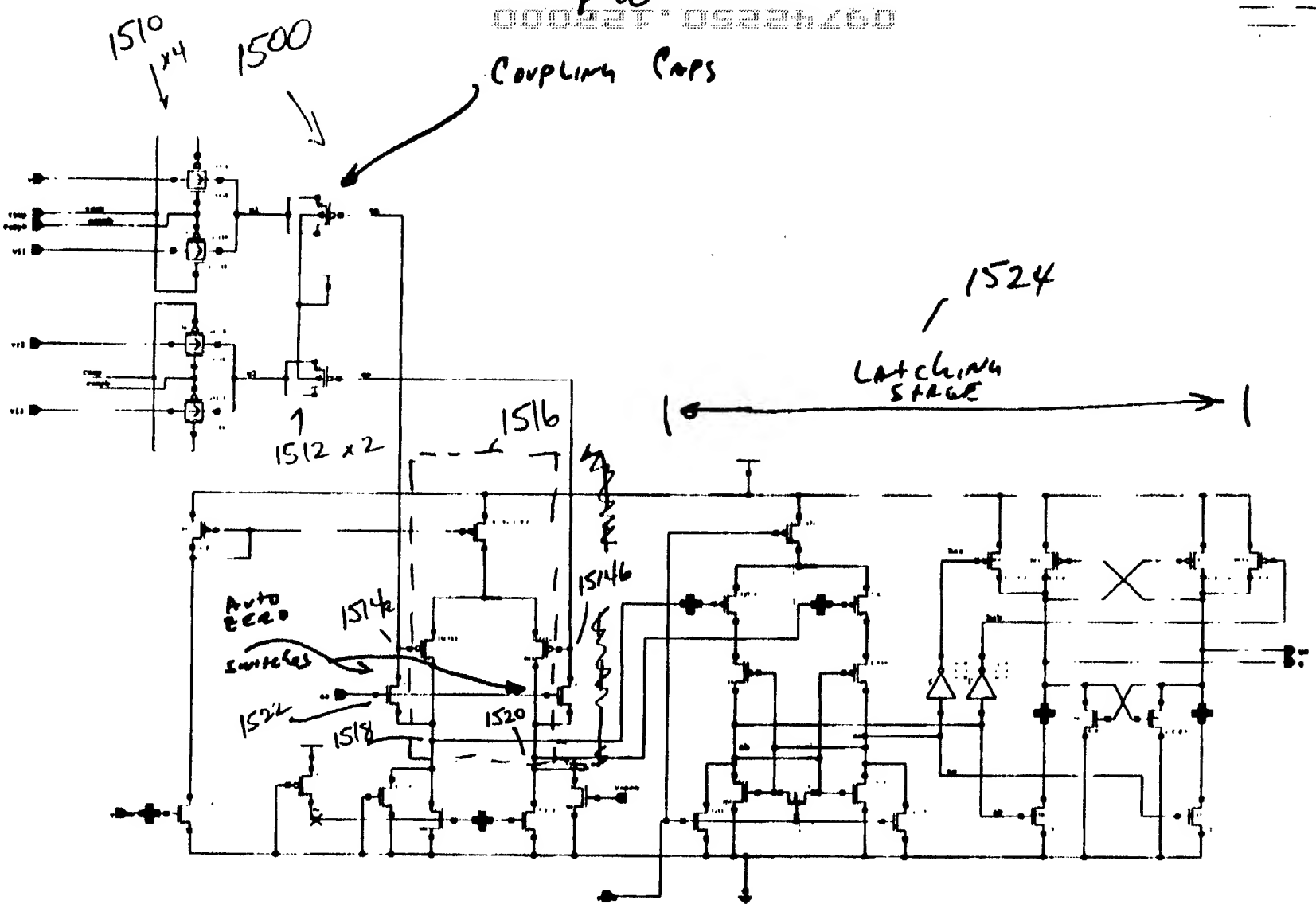

1504
1502
1500
1532
SIGNAL 1506 FROM CALIBRATED DRIVER
1508
SIGNAL FROM DRIVER IN CALIBRATION
NON-OVERLAPING CLOCK DRIVER
STROBE SIGNALS

Fig 13B


1510
x4
1500
Coupling Caps
1524
Latching Stage
1516
1512 x2
1514b
1514a
Auto Zero switches
1522
1518
1520

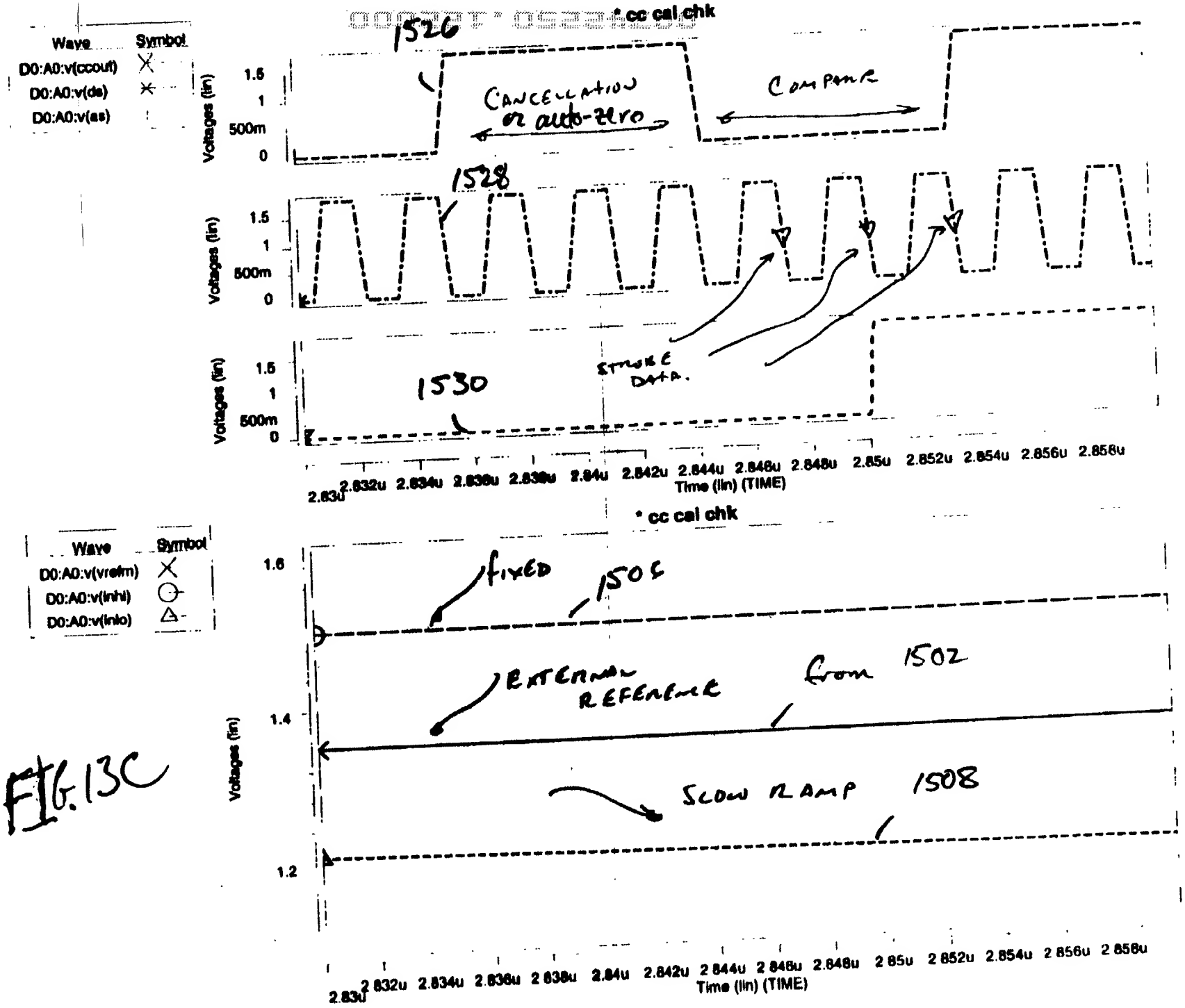
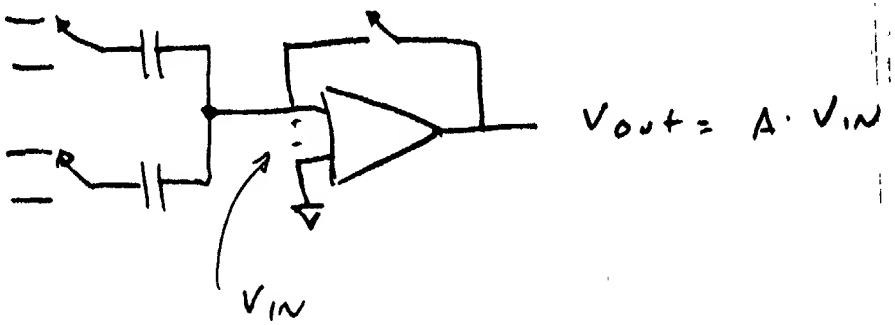

* cc cal chk
Wave
Symbol
D0:A0:v(ccout)
D0:A0:v(ds)
D0:A0:v(as)
Voltages (lin)
1.5
1
500m
0
1526
CANCELLATION or auto-zero
COMPARE
1528
1530
STROBE DATA.
2.83u
2.832u
2.834u
2.836u
2.838u
2.84u
2.842u
2.844u
2.846u
2.848u
2.85u
2.852u
2.854u
2.856u
2.858u
Time (lin) (TIME)
* cc cal chk
Wave
Symbol
D0:A0:v(vrefm)
D0:A0:v(inhi)
D0:A0:v(inlo)
1.6
1.4
1.2
FIXED
1506
EXTERNAL REFERENCE
From 1502
SLOW RAMP
1508

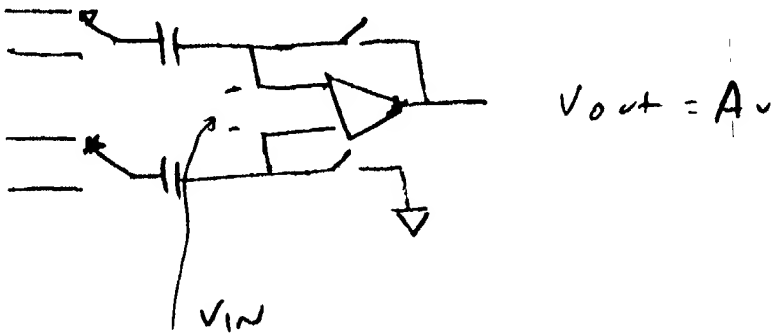
FIG. 13C

ALTERNATE EMBODIMENTS
of DIFFERENTIAL [redacted]
COMPARISONS

FIG. 13D



DIFFERENTIAL IN
SINGLE ENDED
OUT



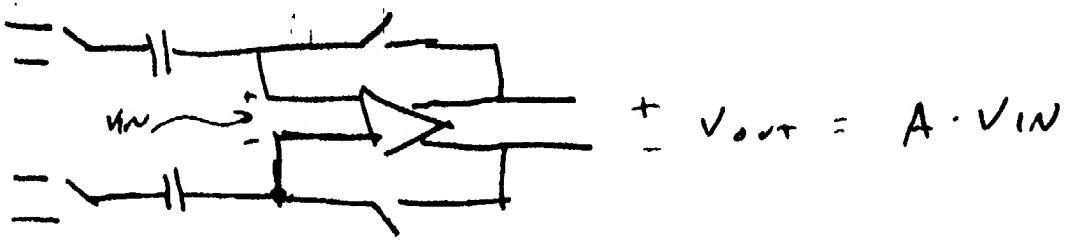


Fig. 13E

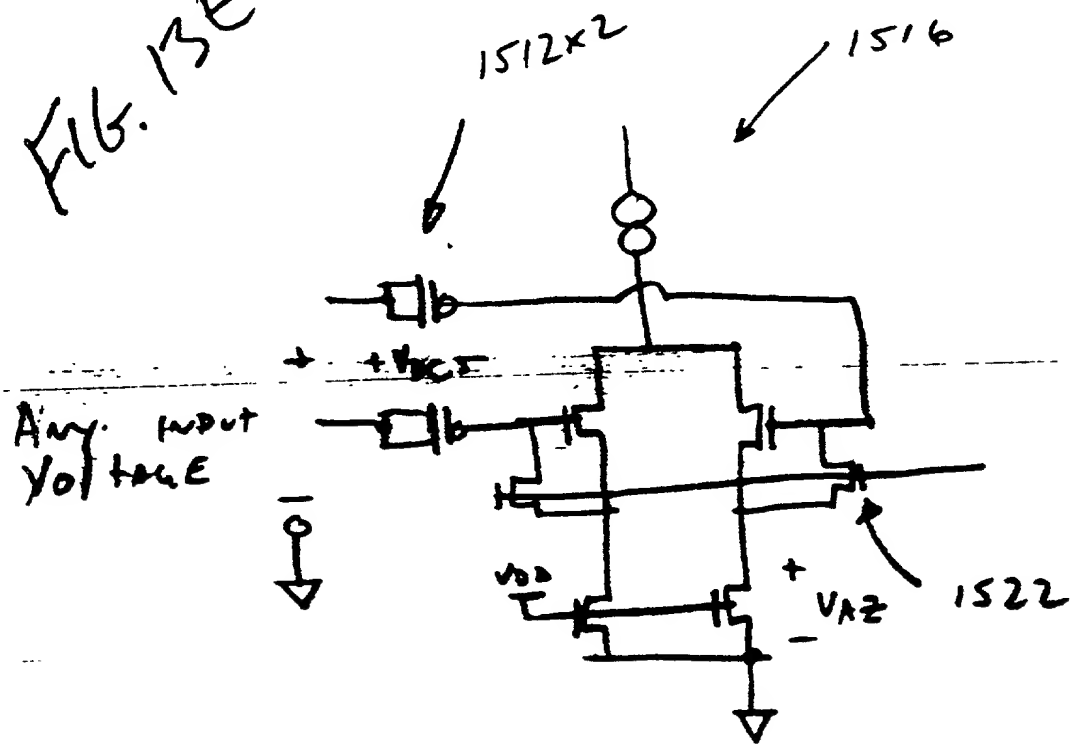


FIG 14A

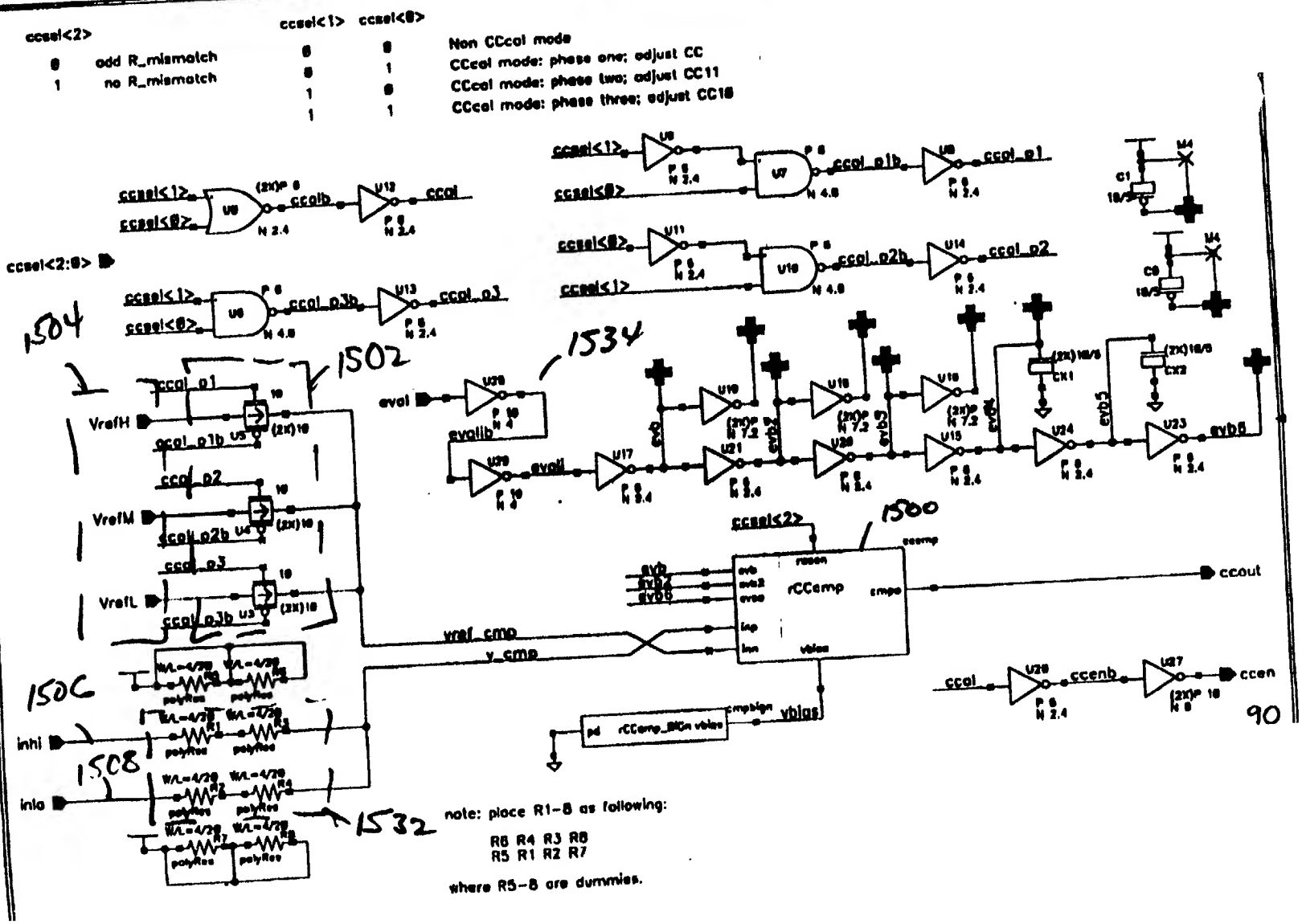

ccsel<2>
0 odd R_mismatch
1 no R_mismatch
ccsel<1> ccsel<0>
0 0 Non CCcal mode
0 1 CCcal mode: phase one; adjust CC
1 0 CCcal mode: phase two; adjust CC11
1 1 CCcal mode: phase three; adjust CC18
ccsel<2:0>
1504
1502
1534
1500
1506
1508
1532
VrefH
VrefM
VrefL
inhi
inlo
ccal_p1
ccal_p1b
ccal_p2
ccal_p2b
ccal_p3
ccal_p3b
evalib
eval
vref_cmp
v_cmp
rCCcmp
ccout
ccen
ccal
ccenb
vblas
note: place R1-8 as following:
R6 R4 R3 R8
R5 R1 R2 R7
where R5-8 are dummies.
90

FIG 14B

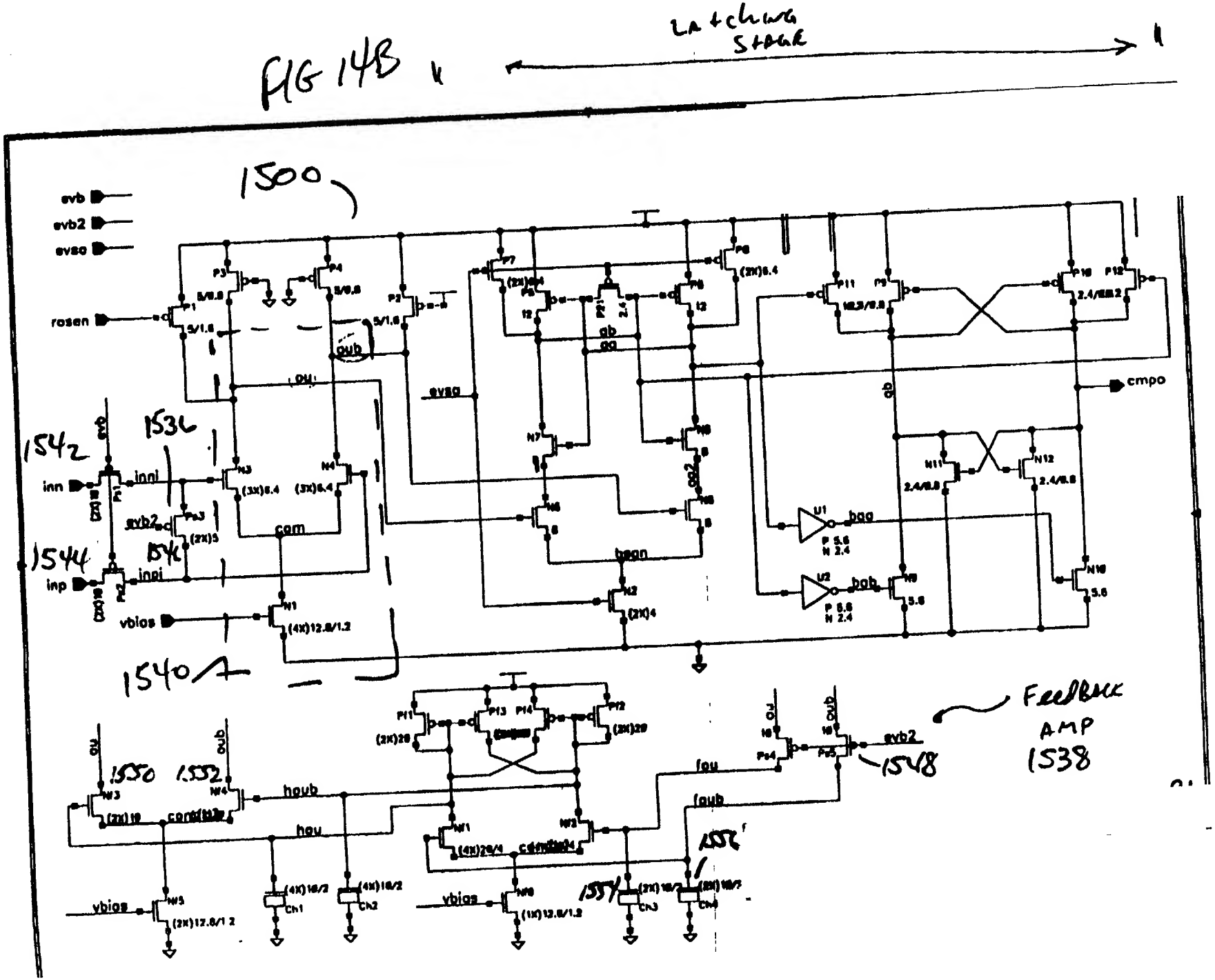

Latching Stage
1500
evb
evb2
evso
rosen
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
qub
qu
evso
gb
gq
cmpo
1542
1536
inn
inni
N3
N4
(3X)6.4
evb2
P13
com
1544
1546
inp
inpi
vbias
N1
(4X)12.8/1.2
1540
N7
N8
N5
N6
gq2
bgqn
N2
(2X)4
U1
bqq
U2
bqb
N9
N10
N11
N12
2.4/0.8
5.6
P 5.6
N 2.4
1550
1552
N13
N14
(2X)10
houb
hou
P11
P12
(2X)20
P13
P14
N11
N12
(4X)20/4
foub
fou
1548
Feedback
AMP
1538
1554
N15
(4X)10/2
Ch1
Ch2
N16
(1X)12.8/1.2
1556
(2X)10/2
Ch3
Ch4

Fig 14C

mismatch w/ os cancellation

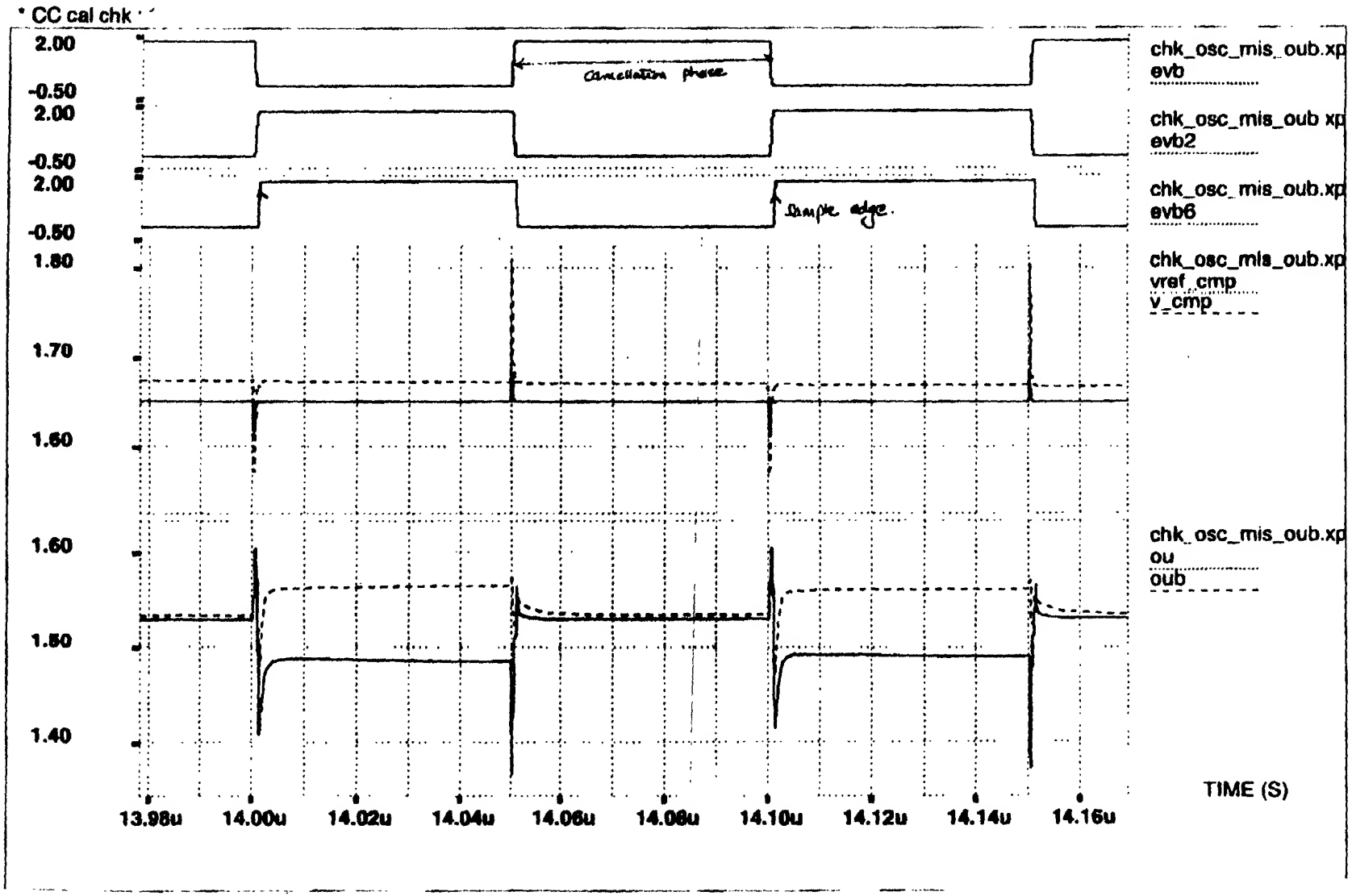


FIG 14D

w/ OS cancel

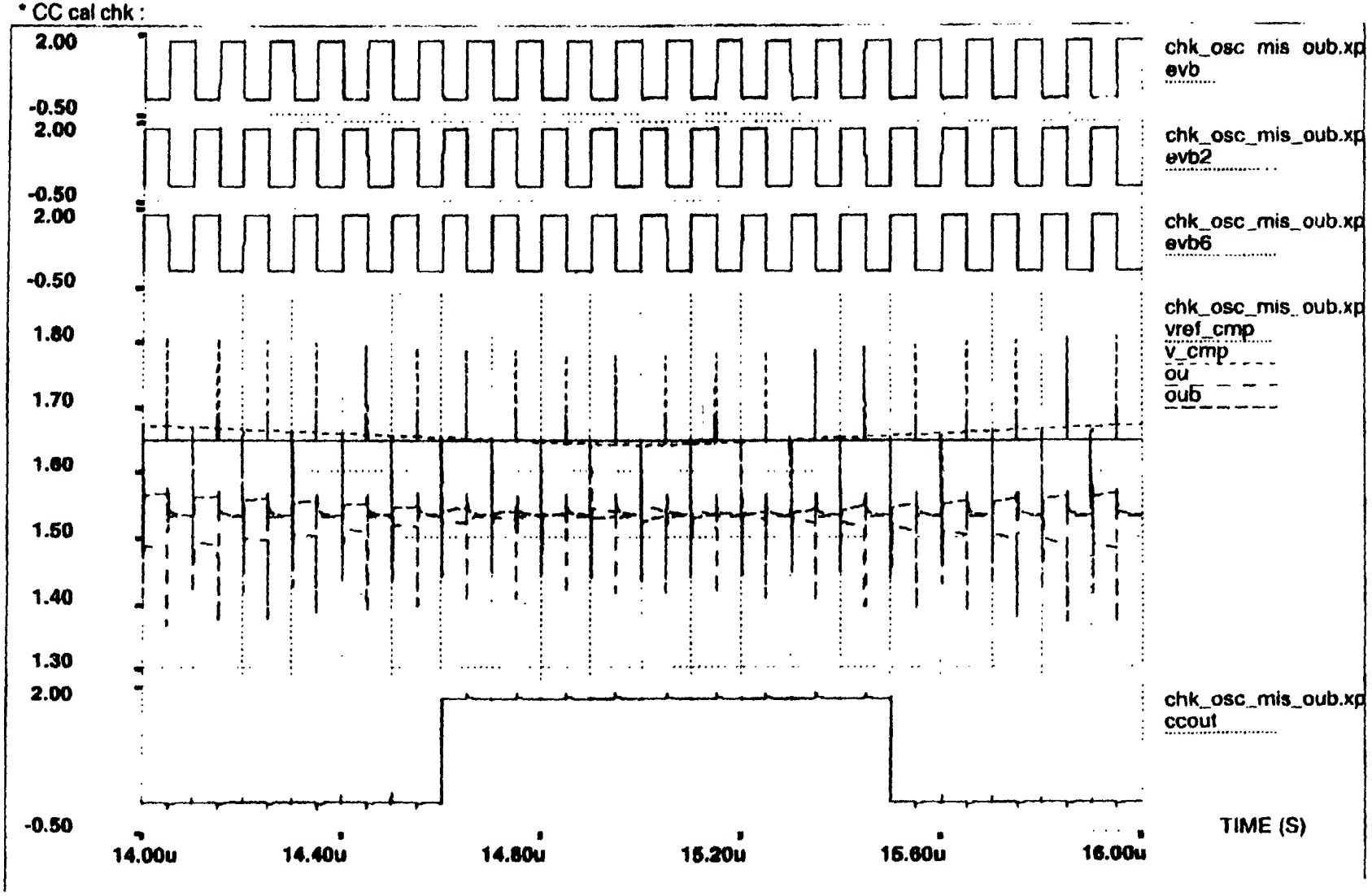
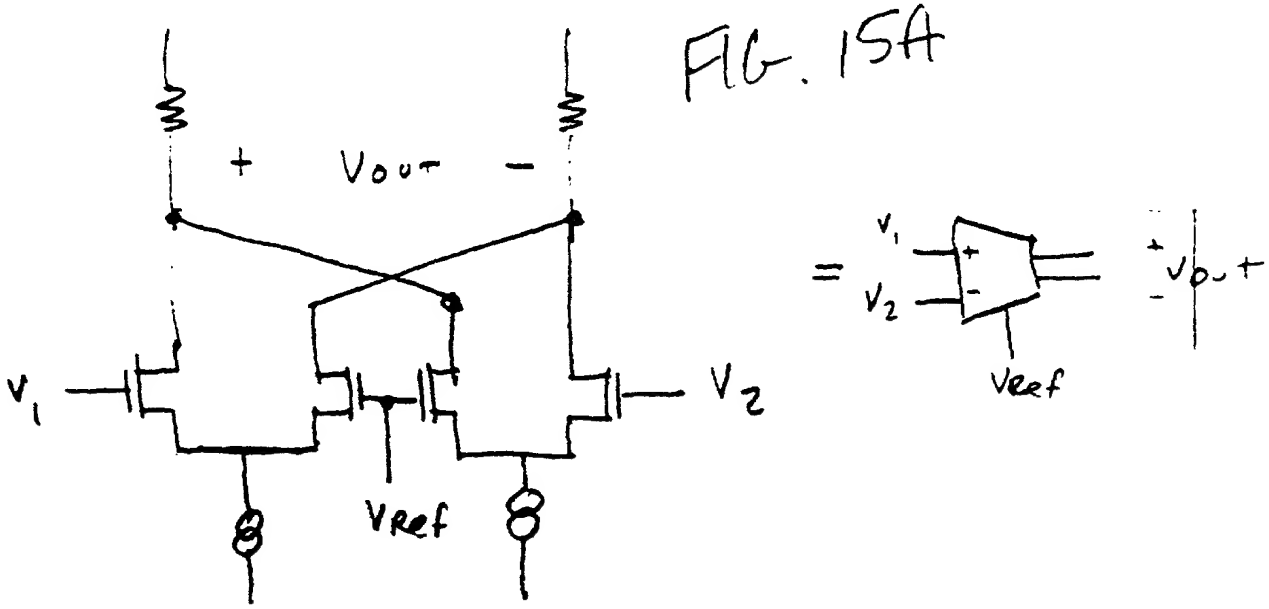


FIG. 15A



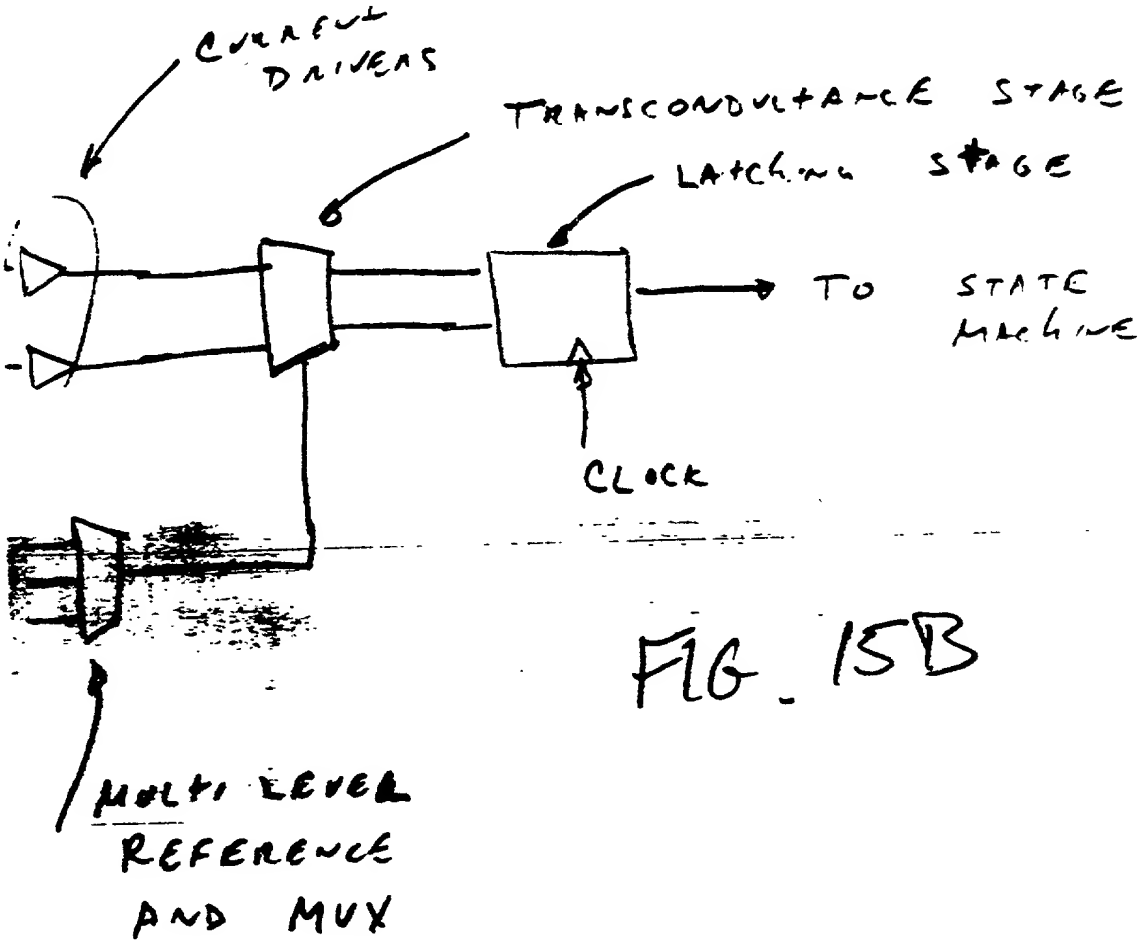

CURRENT DRIVERS
TRANSCONDUCTANCE STAGE
LATCHING STAGE
TO STATE MACHINE
CLOCK
MULTI LEVEL REFERENCE AND MUX

FIG. 15B

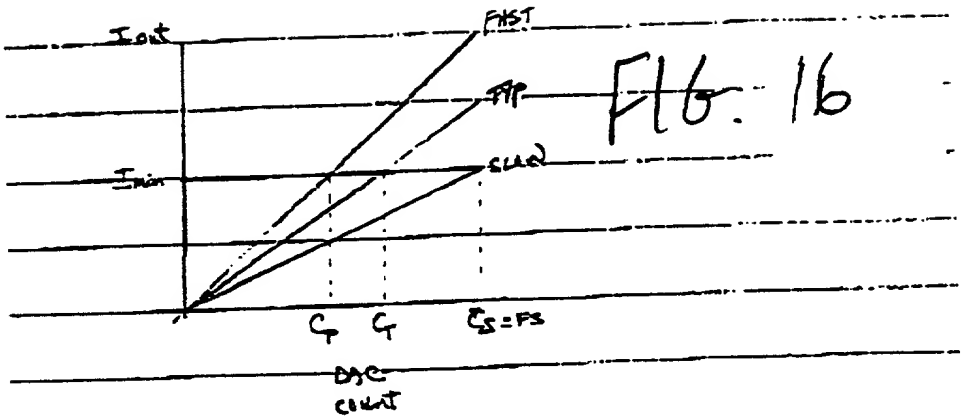


FIG. 16

Output driver block diagram:

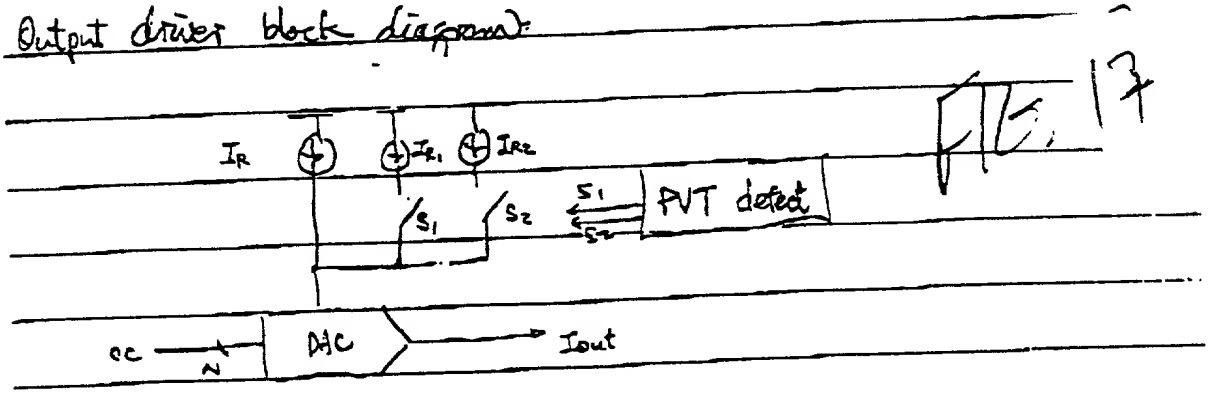
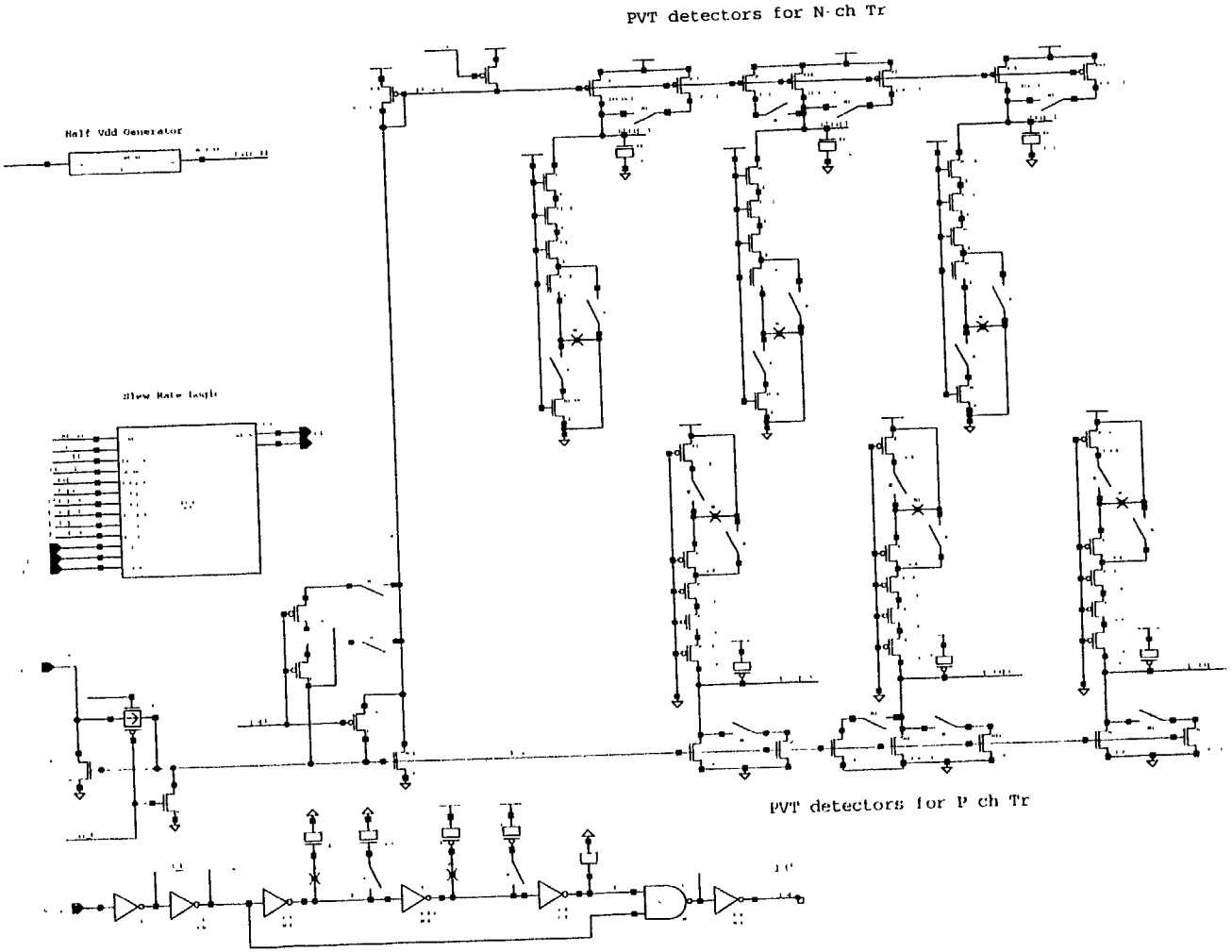


FIG. 17

FIG. 18


PVT detectors for N-ch Tr
Half Vdd Generator
Slew Rate Logic
PVT detectors for P ch Tr

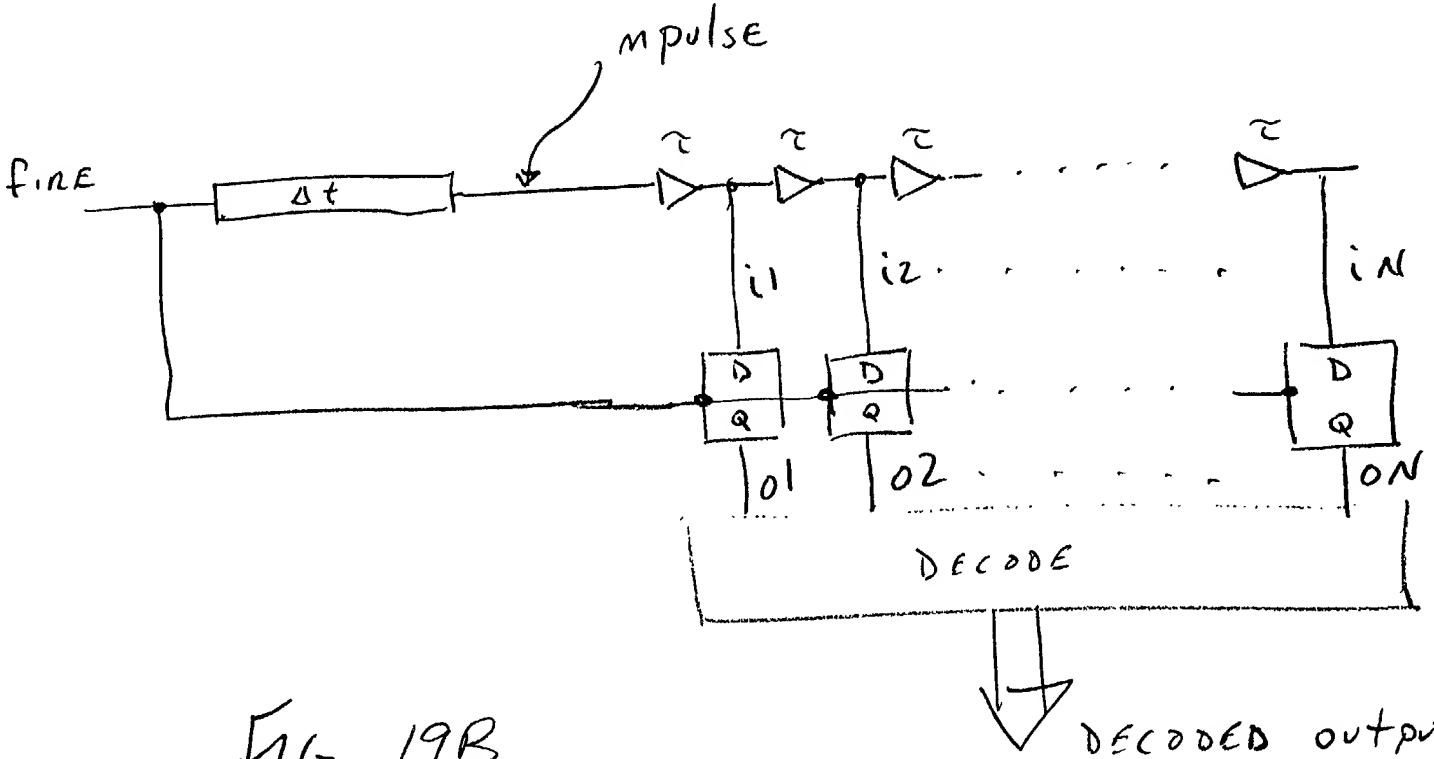


FIG. 19A

FIG. 19B

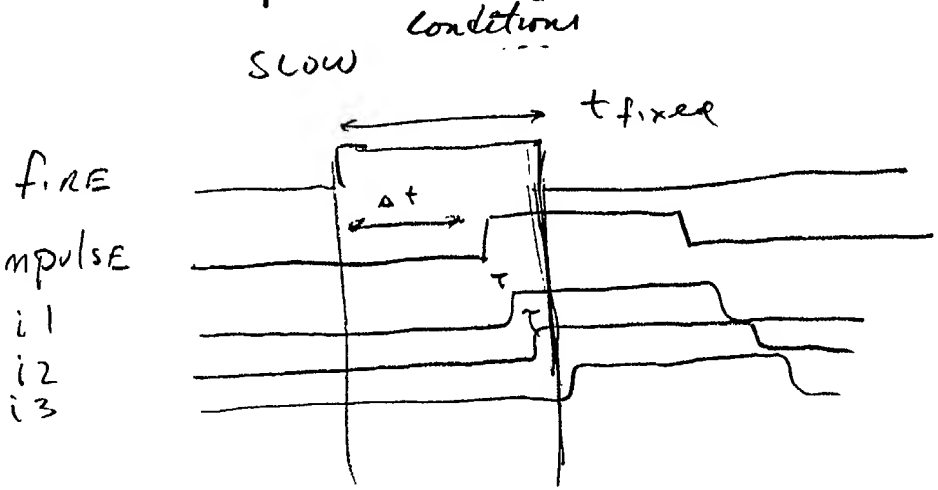


FIG 19C

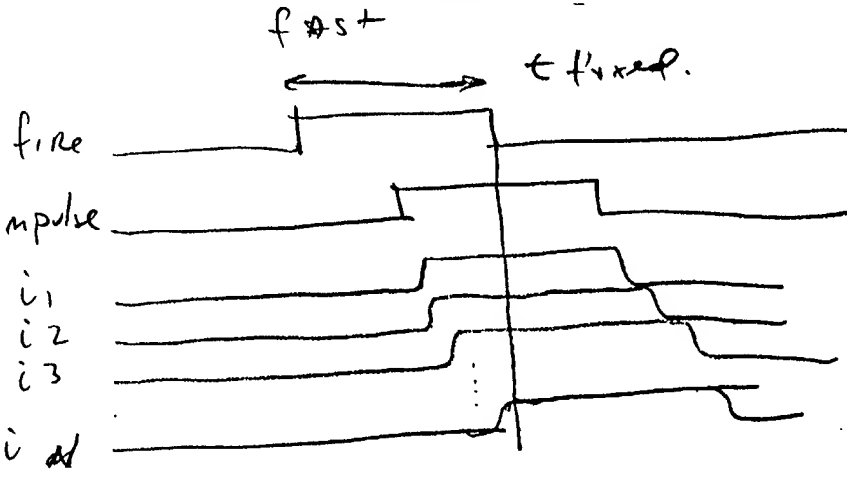
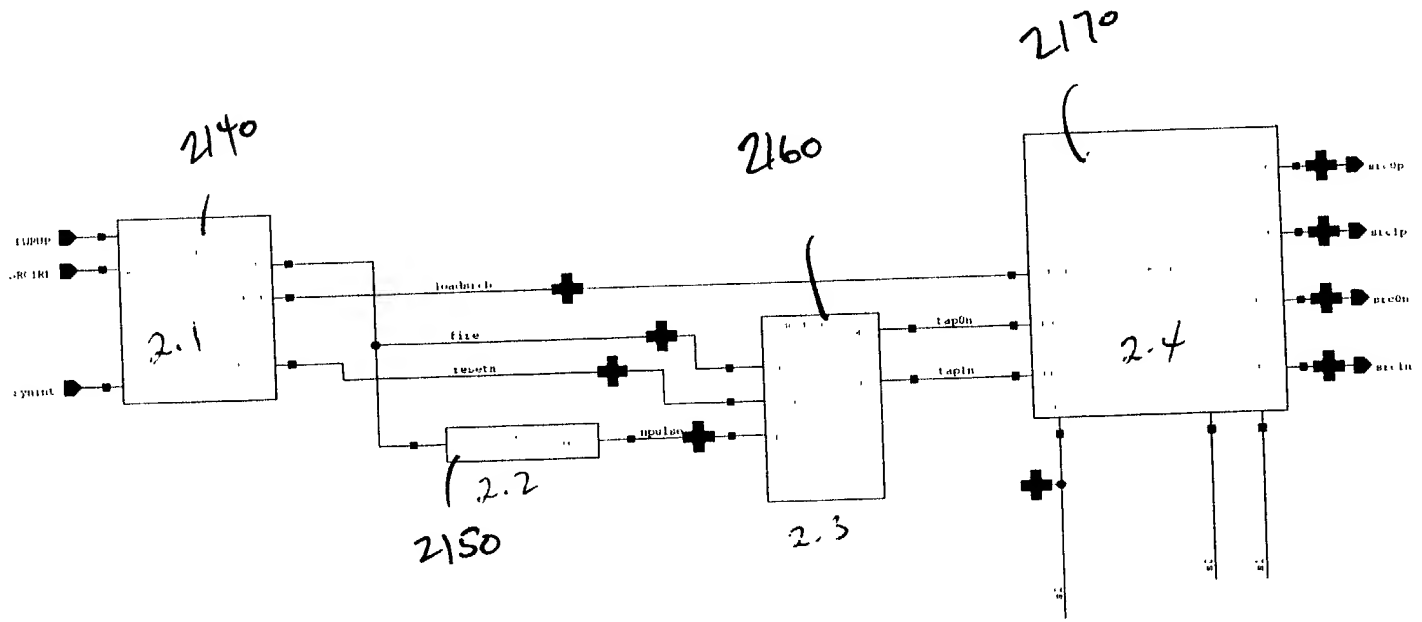


FIG 20A



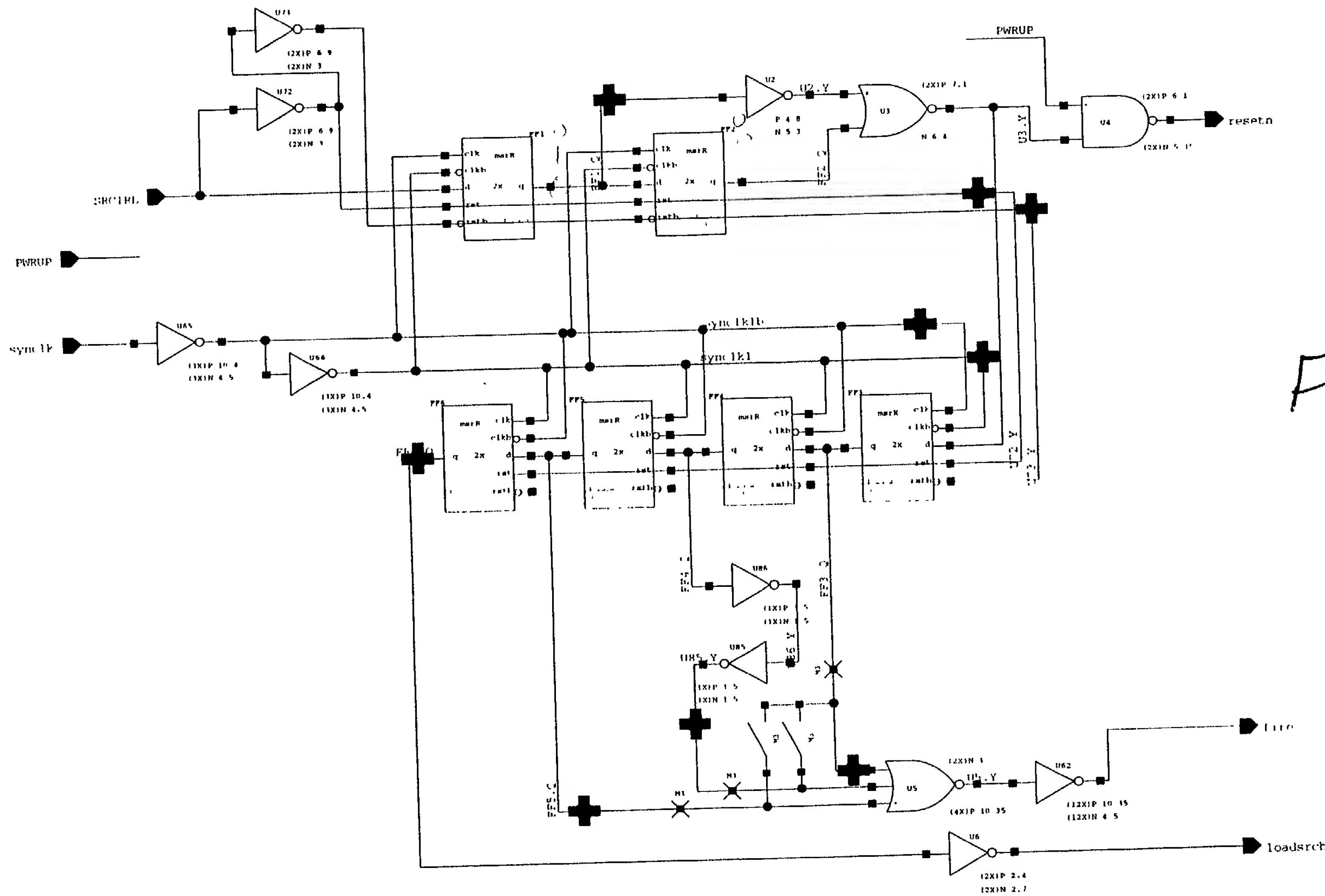

PWRUP
resetn
SRCTRL
PWRUP
synclk
synclk1b
synclk1
U2.Y
U3.Y
U5.Y
U85.Y
U71
U72
U2
U3
U4
U5
U6
U62
U64
U65
U85
U86
clk
clkb
d
set
setb
q
2x
fire
loadsrch

FIG 20B

FIG 20C

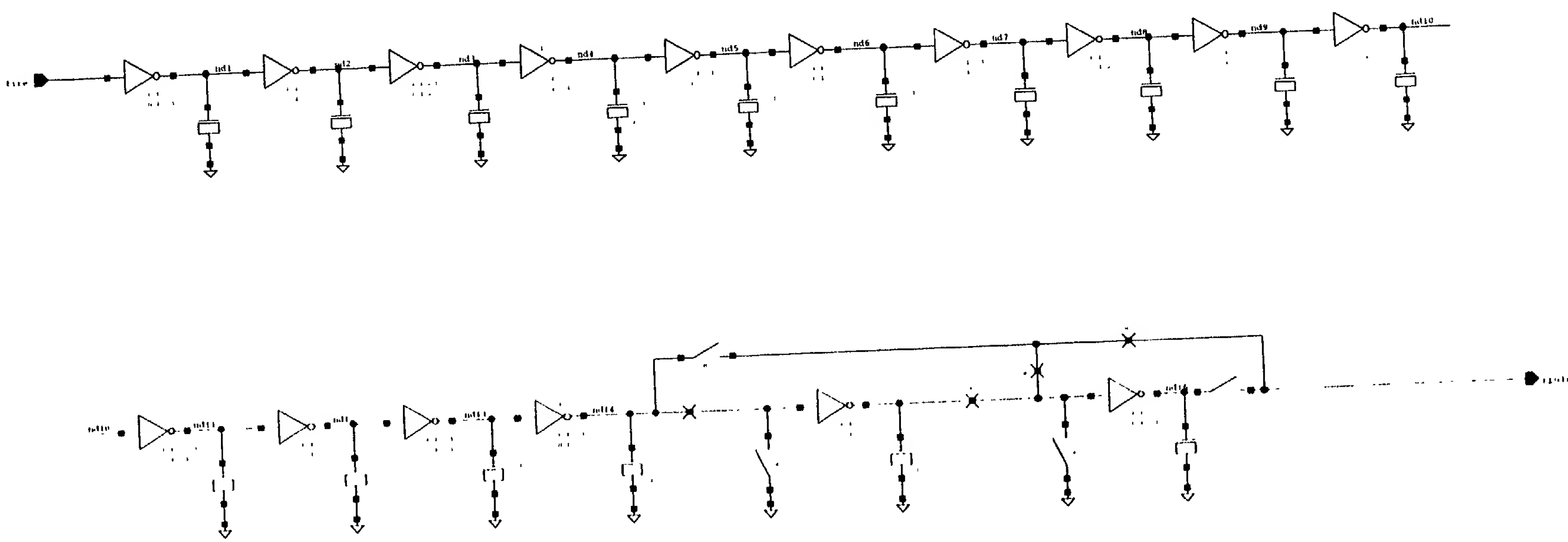


FIG. 20D

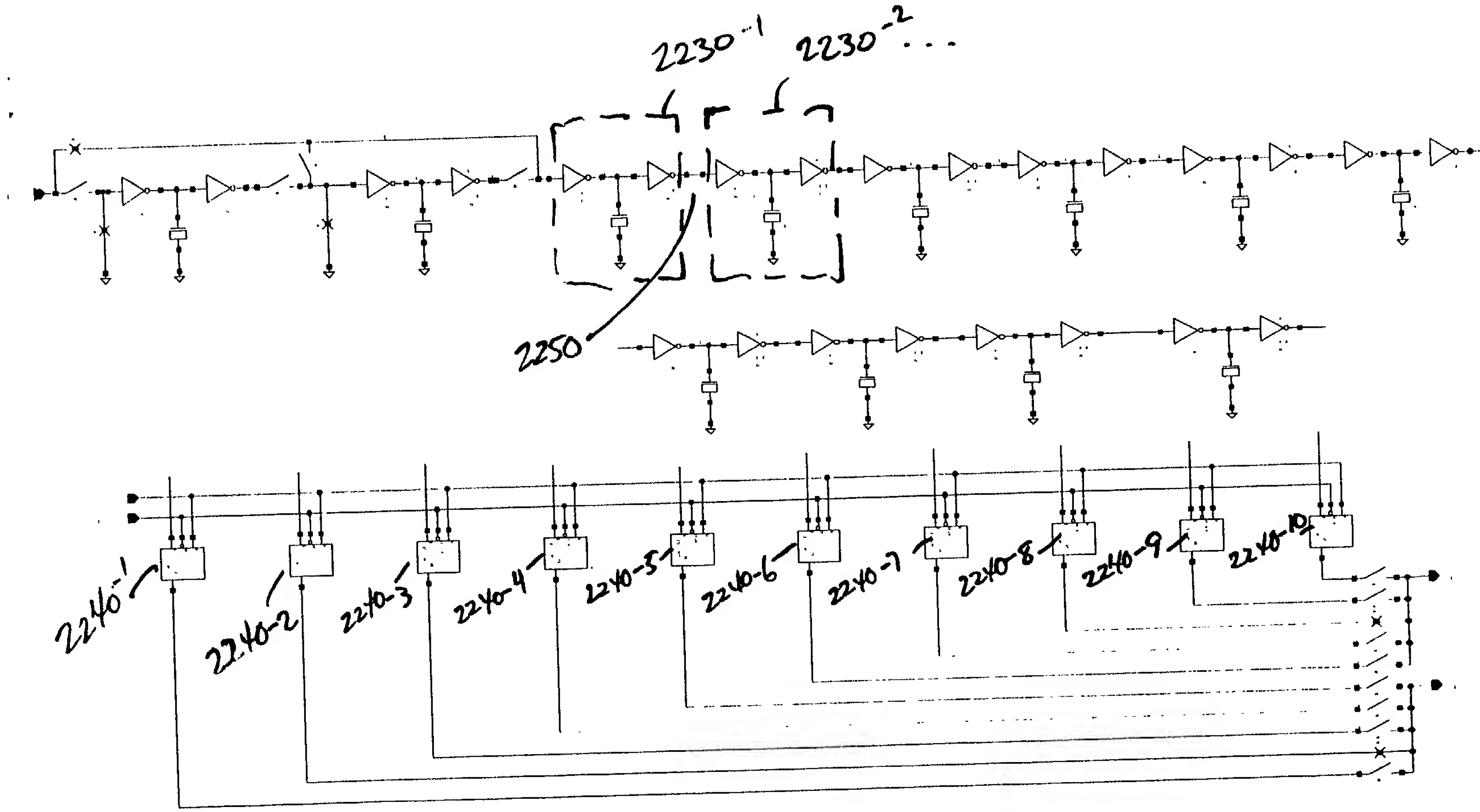
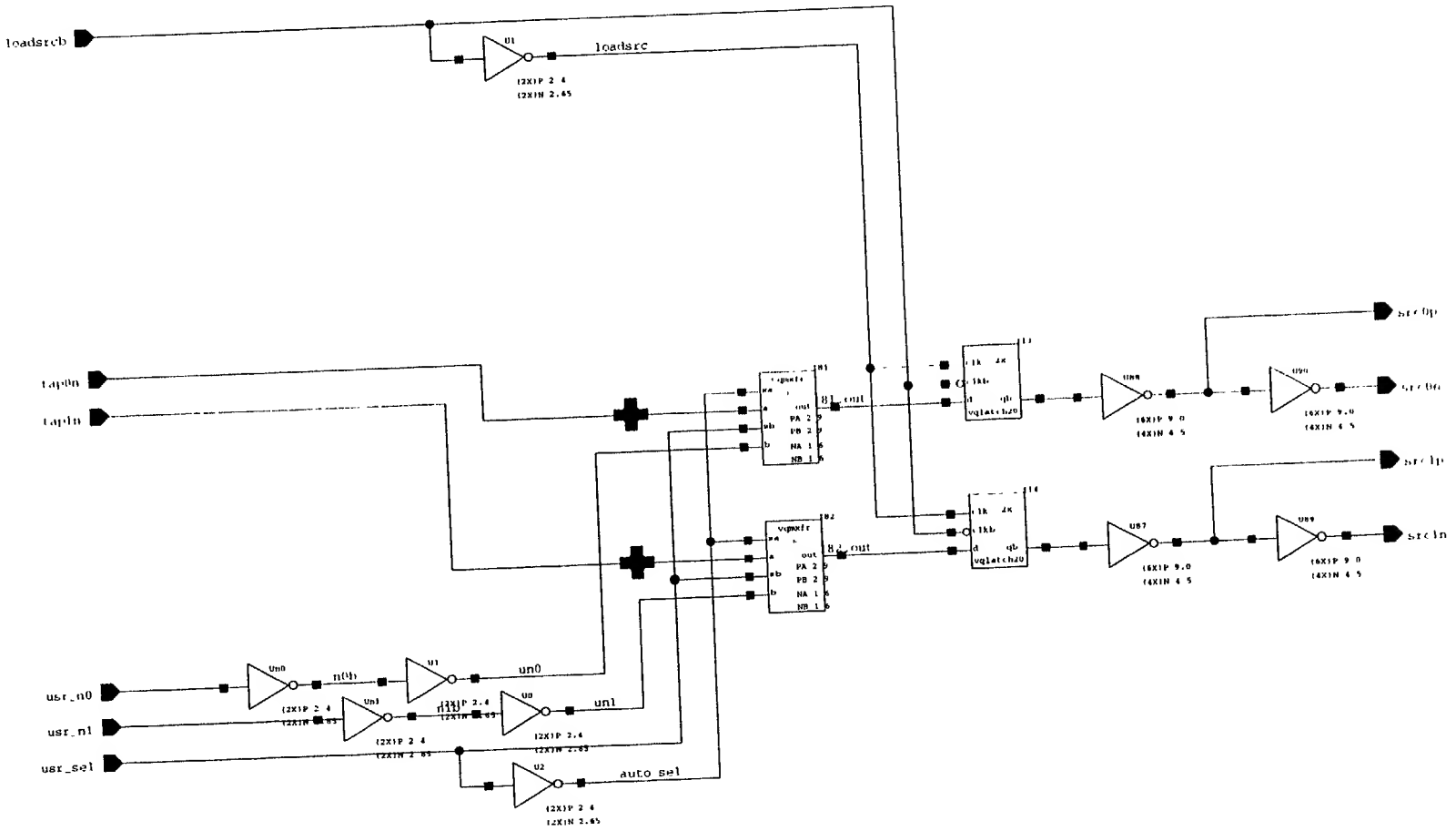

2230-1
2230-2 ...
2250
2240-1
2240-2
2240-3
2240-4
2240-5
2240-6
2240-7
2240-8
2240-9
2240-10

FIG 20E


loadsrcb
loadsrc
tapOn
tapIn
usr_n0
usr_n1
usr_sel
n0
n1
un0
un1
auto_sel
srcOp
srcOn
srcIp
srcIn
out
vqlatch20

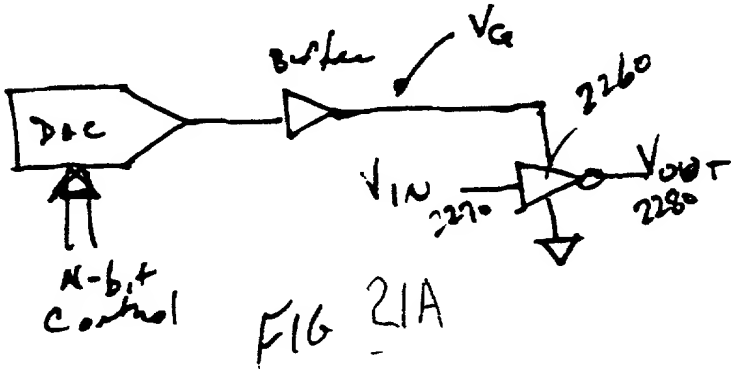


FIG 21A

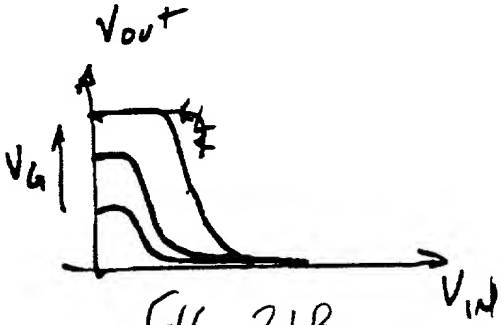


FIG 21B

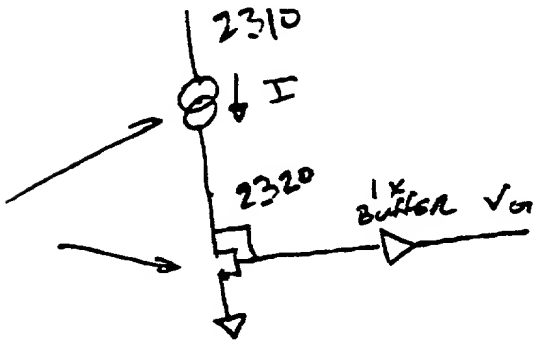


FIG 22

ALTERNATE EMBODIMENT of VGATE DAC

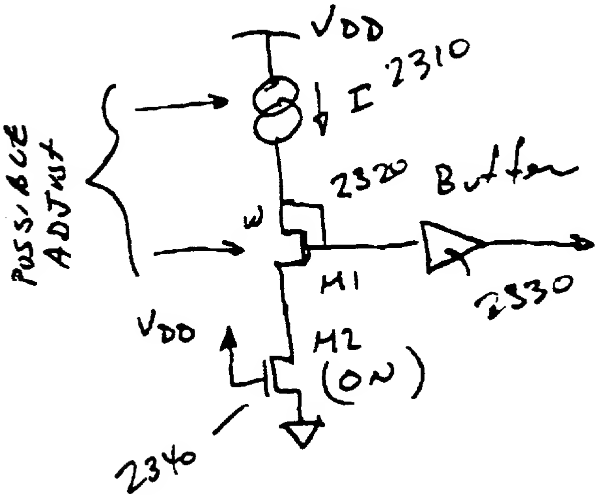


FIG. 23

M1, M2 SCALED to match actual output DRIVER.

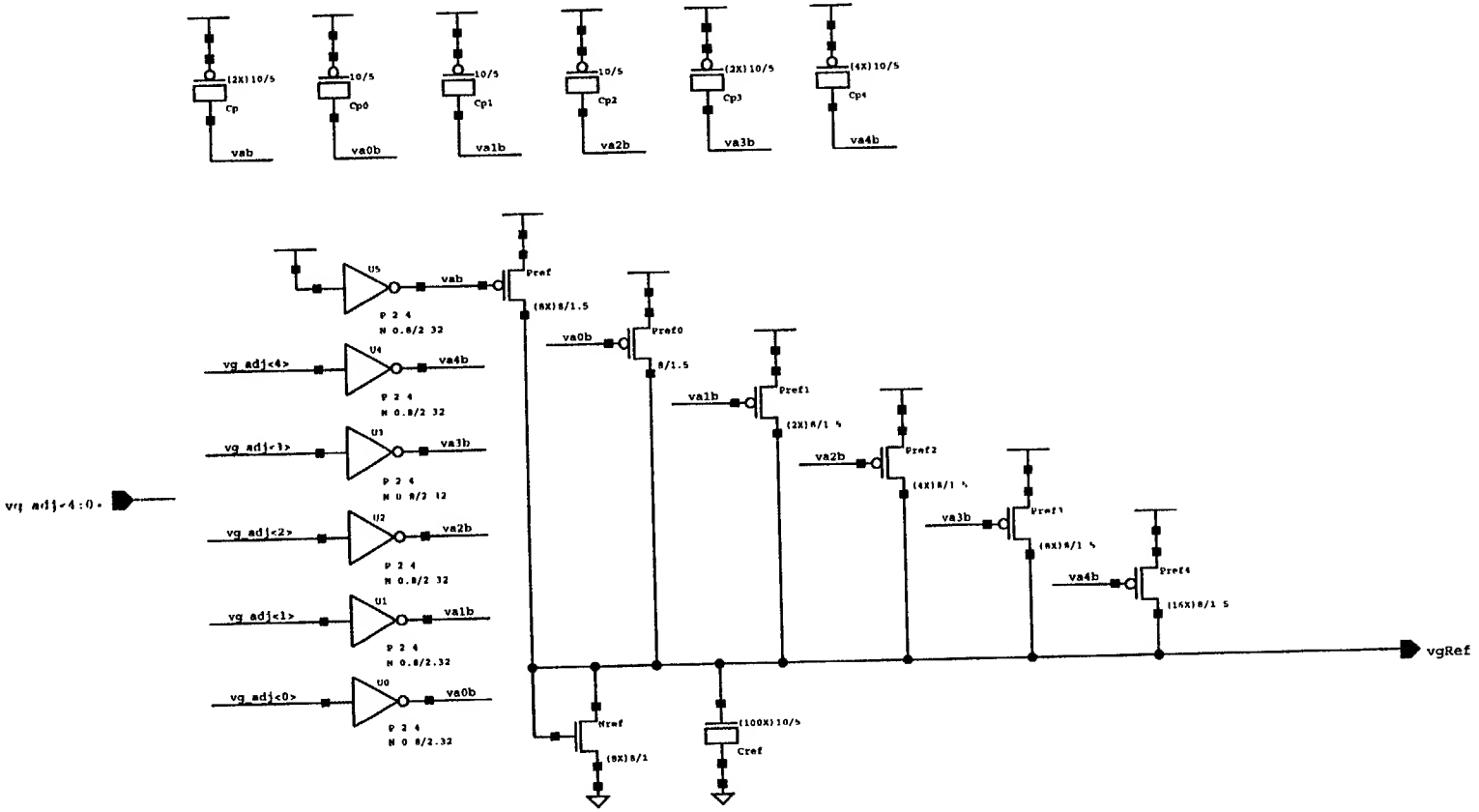

Cp
Cp0
Cp1
Cp2
Cp3
Cp4
vab
va0b
va1b
va2b
va3b
va4b
vg_adj<4:0>
vg_adj<4>
vg_adj<3>
vg_adj<2>
vg_adj<1>
vg_adj<0>
U5
U4
U3
U2
U1
U0
Pref
Pref0
Pref1
Pref2
Pref3
Pref4
Nref
Cref
vgRef

FIG. 24A

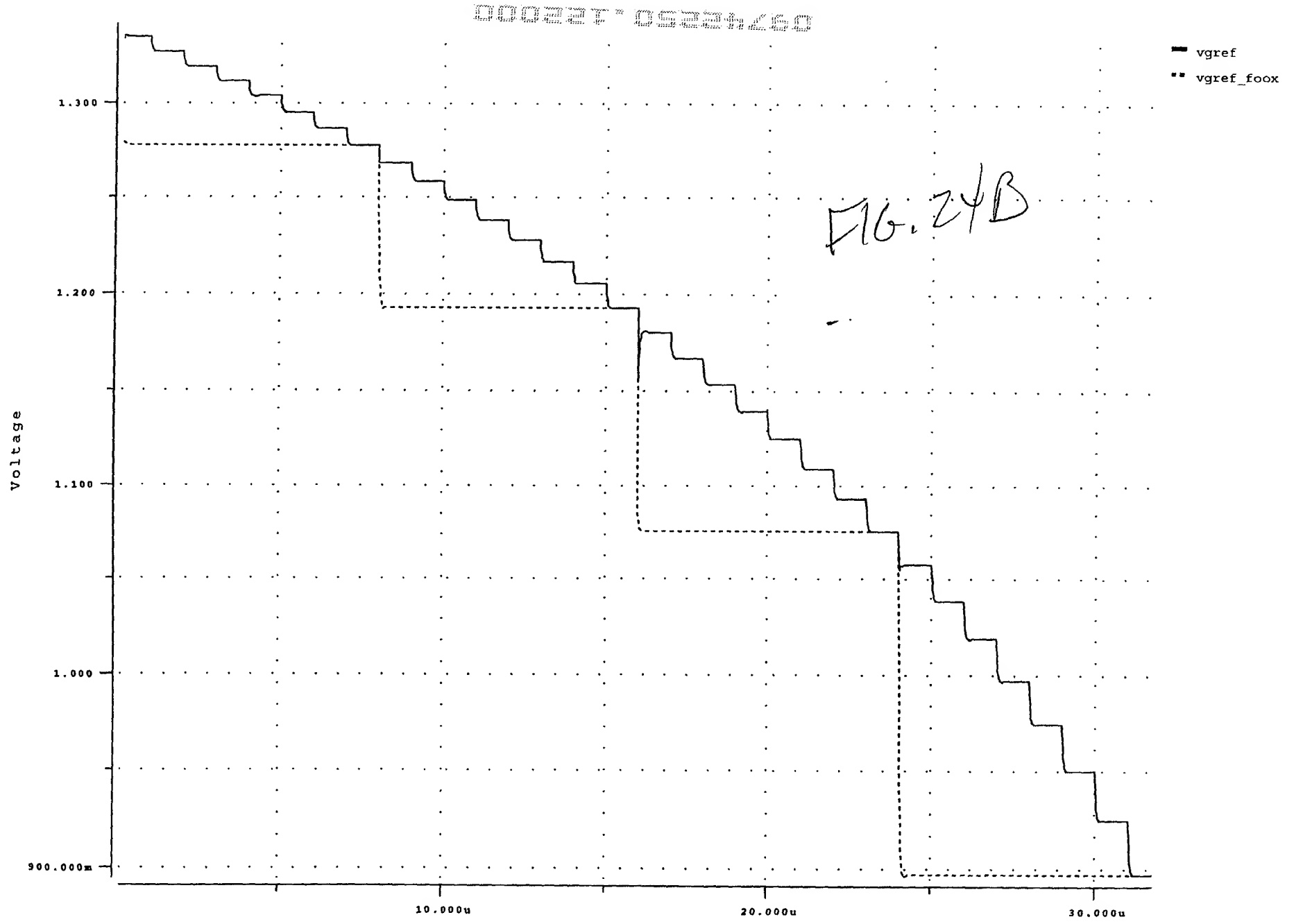

vgref
vgref_foox
1.300
1.200
1.100
1.000
900.000m
Voltage
10.000u
20.000u
30.000u

FIG. 24B